Indra Ganesan
COLLEGE OF ENGINEERING

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai
Accredited by NAAC with 'B+' Grade, 2(f) & 12B Status Institution by UGC

IG Valley, Madurai Main Road, Manikandam, Tiruchirappalli - 620012

NAAC DOCUMENTS

QUALITY INDICATOR FRAME WORK

CRITERION – 2

TEACHING-LEARNING AND EVALUATION

SUBMITTED BY

IQAC

INTERNAL QUALITY ASSURANCE CELL

INDRA GANESAN COLLEGE OF ENGINEERING

Criteria 2	Teaching-Learning and Evaluation	350

Key Indicator-2.6 Student Performances and Learning Outcome (90)

2.6.1 Programme Outcomes (POs) and Course Outcomes (COs) for all programmes offered by the institution are stated and displayed on website

DEPARTMENT OF ME - VLSI DESIGN...R2021

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E . – VLSI DESIGN

REGULATION -2021

COURSE OUTCOMES

SEM –I

C101 VL4153 - Graph Theory and Optimization Techniques

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C101.1	Apply graph ideas is solving connectivity related problems	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C101.2	Apply fundamental graph algorithms to solve certain optimization problems	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C101.3	Formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C101.4	Conceptualize the principle of optimality and sub-optimization, formulation and computational procedure of dynamic programming	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C101.5	Model various real life situations as optimization problems and effect their solution through Non-linear programming	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C101.6	Apply simulation modeling techniques to problems drawn from industry management and other engineering fields	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
C101.1	2	1	1	1	3	3	3	3	3	3	2	2	1	2	2
C101.2	2	1	1	1	3	3	3	3	3	3	2	2	1	2	2
C101.3	2	1	1	1	3	3	3	3	3	3	2	2	1	2	2
C101.4	2	1	1	1	3	3	3	3	3	3	2	2	1	2	2
C101.5	2	1	1	1	3	3	3	3	3	3	2	2	1	2	2
C101.6	2	1	1	1	3	3	3	3	3	3	2	2	1	2	2
C101	3	3	0	2	2	-	-	-	-	-	2	1	-		-

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

C102- RM4151 RESEARCH METHODOLOGY AND IPR

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C102.1	Ability to arrange the conditions for collection and analysis of data in a manner that aims to combine relevance to the research purpose	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C102.2	Ability to gather information in a measured and systematic manner to ensure accuracy and facilitate data analysis	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C102.3	Ability to transform and model the collected data to discover useful information for decision making	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C102.4	Ability to awareness about the benefits of Intellectual property	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C102.5	Ability to take up legal certainty while applying for Patent.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C102.6	create public awareness about the benefits of Intellectual property among students	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
C102.1	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1
C102.2	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1
C102.3	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1
C102.4	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1
C102.5	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1
C102.6	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1
C102	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**1**	**1**	**1**

C103- VL4151 Analog IC Design

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C103.1	Design amplifiers to meet user specifications	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C103.2	Analyse the frequency and noise performance of amplifiers	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C103.3	Design and analyse feedback amplifiers and one stage op amp	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C103.4	Design and analyse two stage op amps	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C103.5	Design and analyse current mirrors and current sinks with mos	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
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	devices		
C103.6	Analyze Stability, frequency response, and Noise in MOS amplifiers	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs,PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C103.1	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1
C103.2	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1
C103.3	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1
C103.4	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1
C103.5	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1
C103.6	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1
C103	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1

C104- VL4152 Digital CMOS VLSI Design

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C104.1	Use mathematical methods and circuit analysis models in analysis of CMOS digital circuits	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C104.2	Create models of moderately sized static CMOS combinational circuits that realize specified digital functions	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C104.3	and to optimize combinational circuit delay using RC delay models and logical effort	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C104.4	Design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C104.5	Understand design methodology of arithmetic building blocks	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C104.6	Design functional units including ROM and SRAM	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C104.1	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C104.2	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C104.3	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
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C104.4	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C104.5	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C104.6	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C104	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2

C105- AP4152 ADVANCED DIGITAL SYSTEM DESIGN

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C105.1	Analyse and design synchronous sequential circuits.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C105.2	Analyse hazards and design asynchronous sequential circuits.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C105.3	Knowledge on the testing procedure for combinational circuit	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C105.4	Knowledge on the testing procedure for PLA.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C105.5	Able to design PLD and ROM.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C105.6	Design and use programming tools for implementing digital circuits of industry standards	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
C105.1	2	2	2	2	1	3	2	3	3	3	3	2	3	2	1
C105.2	2	2	2	2	1	3	2	3	3	3	3	2	3	2	1
C105.3	2	2	2	2	1	3	2	3	3	3	3	2	3	2	1
C105.4	2	2	2	2	1	3	2	3	3	3	3	2	3	2	1
C105.5	2	2	2	2	1	3	2	3	3	3	3	2	3	2	1
C105.6	2	2	2	2	1	3	2	3	3	3	3	2	3	2	1
C105	**2**	**2**	**2**	**2**	**1**	**3**	**2**	**3**	**3**	**3**	**3**	**2**	**3**	**2**	**1**

C106- AP4153 SEMICONDUCTOR DEVICES AND MODELING

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C106.1	Explore the properties of MOS capacitors.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

C106.2	Analyze the various characteristics of MOSFET devices.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C106.3	Describe the various CMOS design parameters and their impact on performance of the device	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C106.4	Discuss the device level characteristics of BJT transistor	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C106.5	Identify the suitable mathematical technique for simulation.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C106.6	design of multistage MOS amplifier and analysis their frequency responses	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
C106.1	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1
C106.2	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1
C106.3	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1
C106.4	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1
C106.5	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1
C106.6	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1
C106	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1

C107- VL4111 FPGA LABORATORY

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C107.1	use the System Verilog RTL design and synthesis features, including new data types, literals, procedural blocks, statements, and operators, relaxation of Verilog language rules, fixes for synthesis issues, enhancements to tasks and functions, new hierarchy	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C107.2	analyse connectivity features, and interfaces. a digital system specification, Map it onto FPGA paltform,	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C107.3	apply the System Verilog verification features, including classes, constrained random stimulus, coverage, strings, queues and dynamic arrays, and learn how to utilize these features for more effective and efficient verification	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C107.4	The implementation of higher level of abstraction to design and verification	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C107.5	Develop Verilog test environments of significant capability and complexity.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C107.6	Integrate scoreboards, multichannel sequencers and Register Models	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

Mapping of COs, PSOs with POs

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C107.1	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C107.2	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C107.3	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C107.4	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C107.5	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C107.6	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C107	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1

C108- VL5201 Design for Verification using UVM

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C108.1	Explainthe basic concepts of two methodologies UVM	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C108.2	build actual verification components	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C108.3	generate the register layer classes.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C108.4	code test benches using UVM.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C108.5	Analyse advanced peripheral bus test benches.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C108.6	provide an experience on self checking UVM testbenches	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
C108. 1	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1
C108. 2	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1
C108. 3	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1
C108. 4	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1
C108. 5	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1
C108. 6	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1
C108	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1

C109 - VL4291 Low Power VLSI Design

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

C109.1	able to find the power dissipation of MOS circuits	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C109.2	design and analyze various MOS logic circuits.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C109.3	apply low power techniques for low power dissipation	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C109.4	able to estimate the power dissipation of ICs	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C109.5	able to develop algorithms to reduce power dissipation by software tools.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C109.6	identify the power reduction techniques based on technology independent and technology dependent methods	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C109.1	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C109.2	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C109.3	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C109.4	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C109.5	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C109.6	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C109	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1

C110- VL5202 LOW POWER VLSI DESIGN

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C110.1	Identify sources of power in an IC	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C110.2	Identify the power reduction techniques based on technology independent and technology	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C110.3	Learn the dependent Power dissipation mechanism in various MOS logic style	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C110.4	Identify suitable techniques to reduce the power dissipation	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C110.5	Design memory circuits with low power dissipation.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C110.6	The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
C110.1	1	1	1	1	2	3	1	1	2	3	1	2	1	1	2
C110.2	1	1	1	1	2	3	1	1	2	3	1	2	1	1	2
C110.3	1	1	1	1	2	3	1	1	2	3	1	2	1	1	2
C110.4	1	1	1	1	2	3	1	1	2	3	1	2	1	1	2
C110.5	1	1	1	1	2	3	1	1	2	3	1	2	1	1	2
C110.6	1	1	1	1	2	3	1	1	2	3	1	2	1	1	2
C110															

C111- VL4292 RF IC Design

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C111.1	Explain the principles of operation of an RF receiver front end	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C111.2	design and apply constraints for LNAs, Mixers	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C111.3	design and apply constraints for frequency synthesizers	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C111.4	analyze and design mixers	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C111.5	design different types of oscillators and perform noise analysis	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C111.6	design PLL and frequency synthesize	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C111.1	1	1	1	1	2	3	1	1	2	3	1	2	1	1
C111.2	1	1	1	1	2	3	1	1	2	3	1	2	1	1
C111.3	1	1	1	1	2	3	1	1	2	3	1	2	1	1
C111.4	1	1	1	1	2	3	1	1	2	3	1	2	1	1
C111.5	1	1	1	1	2	3	1	1	2	3	1	2	1	1
C111.6	1	1	1	1	2	3	1	1	2	3	1	2	1	1
C111	1	1	1	1	2	3	1	1	2	3	1	2	1	1

C112 - VL4252 VLSI Testing

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs

C112.1	Explain the VLSI Testing Process	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C112.2	Develop Logic Simulation and Fault Simulation	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C112.3	Develop Test for Combinational and Sequential Circuits	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C112.4	Explain the Design for Testability.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C112.5	Perform Fault Diagnosis.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C112.6	Learn test generation for combinational logic circuits.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C112.1	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2
C112.2	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2
C112.3	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2
C112.4	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2
C112.5	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2
C112.6	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2
C112	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2

C113- EL4071 Electromagnetic Interference and Compatibility

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C113.1	Demonstrate knowledge of the various sources of electromagnetic interference.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C113.2	Display an understanding of the effect of how electromagnetic fields couple through apertures, and solve simple problems.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C113.3	Explain the EMI mitigation techniques of shielding .	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C113.4	Explain the EMI mitigation techniques of grounding.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C113.5	Explain the need for standards and EMC measurement methods.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C113.6	Discuss the impact of EMC on wireless and broadband technologies.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

C113.1	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2
C113.2	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2
C113.3	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2
C113.4	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2
C113.5	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2
C113.6	2	2	2	2	1	3	2	3	3	3	3	3	3	1	2
C113	**2**	**2**	**2**	**2**	**1**	**3**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**2**

C114 - II4092 System On Chip

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C114.1	Explain all important components of a System-on-Chip.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C114.2	Explain all important components of an embedded system, digital hardware and embedded software	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C114.3	Outline the major design flows for digital hardware	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C114.4	Outline the major design flows for embedded software	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C114.5	Discuss the major architectures and trade-offs concerning performance, cost and power	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C114.6	consumption of single chip and embedded systems;	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C114.1	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C114.2	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C114.3	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C114.4	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C114.5	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C114.6	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C114	**1**	**1**	**1**	**1**	**1**	**3**	**3**	**3**	**2**	**2**	**2**	**2**	**2**	**2**	**1**

C115- VL4211 Verification using UVM Laboratory

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C115.1	Explain the features and capabilities of the UVM class library for system Verilog combine multiple UVCs into a complete verification environment	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.2	create and configure reusable, scalable, and robust UVM verification components (UVCs)	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.3	create a UVM test bench structure using the UVM library base classes and the UVM factory	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.4	develop a register model for your DUT	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.5	use the model for initialization and accessing DUT registers	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.6	design the system with verilog and system Verilog	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C115.1	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.2	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.3	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.4	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.5	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.6	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1

C115- VL4212 Term Paper Writing and Seminar

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C115.1	develop their scientific and technical reading and writing skills that they need to understand and construct research articles	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.2	obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.3	Selection of area of interest and Topic	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.4	Stating an in writing Objective	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.5	Collecting Information about your area & topic	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.6	place it in logically developed ideas.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3

C115.1	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.2	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.3	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.4	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.5	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.6	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115	**1**	**1**	**1**	**1**	**1**	**3**	**3**	**3**	**2**	**2**	**2**	**2**	**2**	**2**	**1**

SEM –III

C201- VL4351 VLSI Signal Processing

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C201.1	determine the parameters influencing the efficiency of DSP architectures.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C201.2	apply pipelining and parallel processing techniques to alter FIR structures for efficiency.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C201.3	analyse and modify the design equations leading to efficient DSP architectures for transforms apply low power techniques for low power dissipation	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C201.4	speed up convolution process and develop fast and area efficient IIR structures	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C201.5	develop fast and area efficient multiplier architectures	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C201.6	reduce multiplications and build fast hardware for synchronous digital systems	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C201. 1	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C201. 2	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C201. 3	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C201. 4	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C201. 5	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C201. 6	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C201	**1**	**1**	**1**	**1**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**1**	**1**

C202- VL4091 Network on Chip

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C202.1	Compare different architecture design	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C202.2	Discuss different routing algorithms	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C202.3	Explain three dimensional Networks on Chip architectures	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C202.4	Test and design fault tolerant NOC	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C202.5	Design three dimensional architectures of NOC	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C202.6	Study fault tolerance Network - on – Chip	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C202.1	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C202.2	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C202.3	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C202.4	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C202.5	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C202.6	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C202	**2**	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**2**	**2**

C203- DS4151 Digital Image and Video Processing

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C203.1	Analyze the digital image, representation of digital image and digital images in transform Domain.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C203.2	Analyze the detection of point, line and edges in images	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C203.3	Explain the redundancy in images, various image compression techniques.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C203.4	Analyze the video technology from analog color TV systems to digital video systems, how video signal is sampled and filtering operations in video processing.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C203.5	Obtain knowledge in general methodologies for 2D motion	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

	estimation, various coding used in video processing.		
C203.6	Design image and video processing systems.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs,PSOs with POs

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C203.1	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C203.2	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C203.3	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C203.4	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C203.5	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C203.6	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C203	**2**	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**2**	**2**

C204- OBA433 INTELLECTUAL PROPERTY RIGHTS

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C204.1	Know the intellectual property and appreciation of the need to protect it	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C204.2	Awareness about the process of patenting	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C204.3	learn the statutes related to IPR	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C204.4	Ability to apply strategies to protect intellectual property	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C204.5	Ability to apply models for making strategic decisions related to IPR	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C204.6	Know the intellectual property rights and its valuation.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 2
C204. 1	2	2	2	2	2	2	3	3	3	3	3	3	2	1	2
C204. 2	2	2	2	2	2	2	3	3	3	3	3	3	2	1	2
C204. 3	2	2	2	2	2	2	3	3	3	3	3	3	2	1	2
C204. 4	2	2	2	2	2	2	3	3	3	3	3	3	2	1	2
C204. 5	2	2	2	2	2	2	3	3	3	3	3	3	2	1	2
C204. 6	2	2	2	2	2	2	3	3	3	3	3	3	2	1	2
C202	**2**	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**1**	**2**

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

C205- VL4311 Project Work I

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C205.1	Research on a topic of interest.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.2	Exposed to self-learning various topics.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.3	Learn to survey the literature such as books, National/ International refereed journals and contact resource persons for the selected topic of research.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.4	Learn to write technical reports.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.5	Develop oral and written communication skills to present	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.6	Prepare the project reports and justify during presentation and demonstration.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C205.1	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.2	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.3	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.4	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.5	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.6	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1

C205- VL4411 Project Work II

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C205.1	Identify challenging practical problems, solutions to cope up with present scenario of electronics field	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.2	Analyze the various methodologies and technologies and discuss with the team for solving the problem.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.3	To develop skills to analyze and discuss the test results, and make conclusions.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

C205.4	On completion of the project work students will be in a position	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.5	To train the students in preparing project reports and to face reviews and viva-voce examination	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.6	At the end of the course the students will have a clear idea of his/her area of work and they are in a position to carry out the remaining phase II work in a systematic way.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C205.1	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.2	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.3	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.4	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.5	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.6	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205	**1**	**1**	**1**	**1**	**1**	**3**	**1**	**3**	**3**	**3**	**2**	**2**	**1**	**1**	**1**

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.