Indra Ganesan
COLLEGE OF ENGINEERING

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai
Accredited by NAAC with 'B+' Grade, 2(f) & 12B Status Institution by UGC

IG Valley, Madurai Main Road, Manikandam, Tiruchirappalli - 620012

NAAC DOCUMENTS

QUALITY INDICATOR FRAME WORK

CRITERION – 2

TEACHING-LEARNING AND EVALUATION

SUBMITTED BY

IQAC

INTERNAL QUALITY ASSURANCE CELL

INDRA GANESAN COLLEGE OF ENGINEERING

Criteria 2	Teaching-Learning and Evaluation	350

Key Indicator-2.6 Student Performances and Learning Outcome (90)

2.6.1 Programme Outcomes (POs) and Course Outcomes (COs) for all programmes offered by the institution are stated and displayed on website

DEPARTMENT OF ME - VLSI DESIGN... R2017

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E . – VLSI DESIGN

REGULATION -2017

COURSE OUTCOMES

SEM –I

C101 MA5152- Applied Mathematics for Electronics Engineers

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C101.1	Concepts of fuzzy sets, knowledge representation using fuzzy rules, fuzzy logic, fuzzy prepositions and fuzzy quantifiers and applications of fuzzy logic.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C101.2	Apply various methods in matrix theory to solve system of linear equations.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C101.3	Computation of probability and moments, standard distributions of discrete and continuous random variables and functions of a random variable.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C101.4	Conceptualize the principle of optimality and sub-optimization, formulation and computational procedure of dynamic programming	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C101.5	Exposing the basic characteristic features of a queuing system and acquire skills in analyzing queuing models.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C101.6	Using discrete time Markov chains to model computer systems.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C101.1	2	1	1	1	3	3	3	3	3	3	2	2	1	2	2
C101.2	2	1	1	1	3	3	3	3	3	3	2	2	1	2	2
C101.3	2	1	1	1	3	3	3	3	3	3	2	2	1	2	2
C101.4	2	1	1	1	3	3	3	3	3	3	2	2	1	2	2
C101.5	2	1	1	1	3	3	3	3	3	3	2	2	1	2	2
C101.6	2	1	1	1	3	3	3	3	3	3	2	2	1	2	2
C101	3	3	0	2	2	-	-	-	-	-	2	1	-		-

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C102- AP5151 ADVANCED DIGITAL SYSTEM DESIGN

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C102.1	Analyze and design synchronous sequential digital circuits	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C102.2	Analyze and design asynchronous sequential circuits	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C102.3	Identify the requirements and specifications of the system required for a given application	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C102.4	Desin the architectures of programmable devices	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C102.5	Analyze the fault diagnosis and testability algorithms	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C102.6	Design and use programming tools for implementing digital circuits of industry standards	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
C102.1	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1
C102.2	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1
C102.3	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1
C102.4	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1
C102.5	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1
C102.6	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1
C102	2	2	2	2	2	3	3	3	2	3	3	2	1	1	1

C103- VL5101 CMOS DIGITAL VLSI DESIGN

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C103.1	Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C103.2	Discuss design methodology of arithmetic building block	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C103.3	Analyze tradeoffs of the various circuit choices for each of the building block.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C103.4	Explain the Arithmetic building blocks and memory architectures	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C103.5	Explain the Interconnect and clocking strategies	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
	Explain the Low Power Design principles.		

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C103.6		1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs,PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C103.1	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1
C103.2	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1
C103.3	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1
C103.4	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1
C103.5	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1
C103.6	2	2	2	2	2	3	3	3	3	3	3	3	1	2	1
C103	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**2**	**1**

C104- VL5191 DSP INTEGRATED CIRCUITS

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C104.1	know about the Digital Signal Processing concepts and its algorithms	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C104.2	Get an idea about finite word length effects in digital filters	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C104.3	Explain the Concept behind multi rate systems	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C104.4	Get familiar with the DSP processor architectures	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C104.5	Analyze how to perform synthesis of processing elements	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C104.6	Explin the Arithmetic unit and CORDIC Algorithm , DCT and FFT processor	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C104.1	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C104.2	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C104.3	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C104.4	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C104.5	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C104.	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2

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C104	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2

C105- VL5102 CAD FOR VLSI CIRCUITS

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C105.1	Learn VLSI Design methodologies	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C105.2	Analyze VLSI design automation tools	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C105.3	Know the modelling and simulation	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C105.4	Design floor planning and routing	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C105.5	Explain Simulation and Logic Synthesis	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C105.6	Discuss the hardware models for high level synthesis	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
C105.1	2	2	2	2	1	3	2	3	3	3	3	2	3	2	1
C105.2	2	2	2	2	1	3	2	3	3	3	3	2	3	2	1
C105.3	2	2	2	2	1	3	2	3	3	3	3	2	3	2	1
C105.4	2	2	2	2	1	3	2	3	3	3	3	2	3	2	1
C105.5	2	2	2	2	1	3	2	3	3	3	3	2	3	2	1
C105.6	2	2	2	2	1	3	2	3	3	3	3	2	3	2	1
C105	**2**	**2**	**2**	**2**	**1**	**3**	**2**	**3**	**3**	**3**	**3**	**2**	**3**	**2**	**1**

C106- VL5103 ANALOG IC DESIGN

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C106.1	Know about MOS devices modelling and scaling effects.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C106.2	design of single stage MOS amplifier and analysis their frequency responses	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C106.3	design of multistage MOS amplifier and analysis their frequency responses	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C106.4	different design parameters in designing voltage reference .	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C106.5	different design parameters in designing OPAMP circuits.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

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C106.6	Analyze Stability, frequency response, and Noise in MOS amplifiers	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
C106. 1	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1
C106. 2	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1
C106. 3	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1
C106. 4	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1
C106. 5	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1
C106. 6	2	2	2	2	1	3	3	3	3	3	3	3	1	2	1
C106	**2**	**2**	**2**	**2**	**1**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**2**	**1**

C107- VL5111 VLSI DESIGN LABORATORY I

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C107.1	given a digital system specification, Map it onto FPGA paltform,	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C107.2	carry out a series of validations design starting from design entry to hardware testing.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C107.3	design and carry out time domain simulations of simple analog building blocks	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C107.4	design and carry out frequency domain simulations of simple analog building blocks	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C107.5	Know the pole zero behaviors of feedback based circuits	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C107.6	compute the input/output impedances.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C107.1	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C107.2	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C107.3	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C107.4	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C107.5	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C107.6	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C107	**1**	**1**	**1**	**1**	**1**	**3**	**3**	**3**	**2**	**2**	**2**	**2**	**2**	**2**	**1**

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C108- VL5201Testing of VLSI Circuits

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C108.1	Analysis the logic fault models.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C108.2	Learn test generation for sequential circuits.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C108.3	Learn test generation for combinational logic circuits.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C108.4	Prepare design for testability.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C108.5	Discuss test algorithms.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C108.6	Explain fault diagnosis.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
C108.1	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1
C108.2	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1
C108.3	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1
C108.4	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1
C108.5	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1
C108.6	2	2	2	2	1	3	2	3	3	3	3	3	3	2	1
C108	**2**	**2**	**2**	**2**	**1**	**3**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**1**

C109 - VL5291 VLSI SIGNAL PROCESSING

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C109.1	Learn the techniques for altering the existing DSP structures to suit VLSI implementations.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C109.2	Learn the techniques efficient design of DSP architectures suitable for VLSI	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C109.3	Ability to modify the existing or new DSP architectures suitable for VLSI.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C109.4	Learn Pipelining and parallel processing of digital filters	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C109.5	Write Algorithmic strength reduction technique	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C109.6	Explain the Numerical strength reduction, wave and asynchronous pipelining	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

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Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
C109. 1	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C109. 2	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C109. 3	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C109. 4	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C109. 5	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C109. 6	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C109	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1

C110- VL5202 LOW POWER VLSI DESIGN

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C110.1	Identify sources of power in an IC	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C110.2	Identify the power reduction techniques based on technology independent and technology	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C110.3	Learn the dependent Power dissipation mechanism in various MOS logic style	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C110.4	Identify suitable techniques to reduce the power dissipation	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C110.5	Design memory circuits with low power dissipation.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C110.6	The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
C110. 1	1	1	1	1	2	3	1	1	2	3	1	2	1	1	2
C110. 2	1	1	1	1	2	3	1	1	2	3	1	2	1	1	2
C110. 3	1	1	1	1	2	3	1	1	2	3	1	2	1	1	2

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C110.4	1	1	1	1	2	3	1	1	2	3	1	2	1	1	2
C110.5	1	1	1	1	2	3	1	1	2	3	1	2	1	1	2
C110.6	1	1	1	1	2	3	1	1	2	3	1	2	1	1	2
C110	**1**	**1**	**1**	**1**	**2**	**3**	**1**	**1**	**2**	**3**	**1**	**2**	**1**	**1**	**2**

C111- VL5002 RF IC Design

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C111.1	Explain the various impedance matching techniques used in RF circuit design.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C111.2	Explain the functional design aspects of LNAs Mixers.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C111.3	Explain the functional design aspects of PLLs and VCO.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C111.4	Explain frequency synthesis.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C111.5	Explain the principles of operation of an RF receiver front end	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C111.6	apply constraints for LNAs, Mixers and Frequency synthesizers	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
C111.1	1	2	1	1	1	3	2	3	3	3	2	3	2	2	2
C111.2	1	2	1	1	1	3	2	3	3	3	2	3	2	2	2
C111.3	1	2	1	1	1	3	2	3	3	3	2	3	2	2	2
C111.4	1	2	1	1	1	3	2	3	3	3	2	3	2	2	2
C111.5	1	2	1	1	1	3	2	3	3	3	2	3	2	2	2
C111.6	1	2	1	1	1	3	2	3	3	3	2	3	2	2	2
C111	**1**	**2**	**1**	**1**	**1**	**3**	**2**	**3**	**3**	**3**	**2**	**3**	**2**	**2**	**2**

C112 - AP5094 Signal Integrity for High Speed Design

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C112.1	Identify sources affecting the speed of digital circuits.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

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C112.2	Introduce methods to improve the signal transmission characteristics.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C112.3	Learn Multi-conductor transmission lines and cross-talk.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C112.4	Learn Non-ideal effects.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C112.5	Explain the Power considerations and system design.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C112.6	Design Clock distribution and clock oscillators.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C112.1	1	1	2	2	1	3	2	3	3	3	3	3	1	2	1
C112.2	1	1	2	2	1	3	2	3	3	3	3	3	1	2	1
C112.3	1	1	2	2	1	3	2	3	3	3	3	3	1	2	1
C112.4	1	1	2	2	1	3	2	3	3	3	3	3	1	2	1
C112.5	1	1	2	2	1	3	2	3	3	3	3	3	1	2	1
C112.6	1	1	2	2	1	3	2	3	3	3	3	3	1	2	1
C112	**1**	**1**	**2**	**2**	**1**	**3**	**2**	**3**	**3**	**3**	**3**	**3**	**1**	**2**	**1**

C113- AP5191 Embedded System Design

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C113.1	Learn design challenges and design methodologies.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C113.2	Study general and single purpose processor.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C113.3	Explain about bus structures.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C113.4	Explain different protocols.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C113.5	Discuss state machine and design process models.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C113.6	Outline embedded software development tools and RTOS.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C113.1	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C113.2	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2

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C113.3	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C113.4	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C113.5	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C113.6	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2
C113	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**2**	**2**

C114 - VL5211 VLSI DESIGN LABORATORY II

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C114.1	Analyze the CAD based VLSI design flow.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C114.2	The entire VLSI design industry makes use of this design flow in some for or the other.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C114.3	Proficiency and familiarity with the various stages of a typical state of this design flow to be apart of either the industry or their search in VLSI	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C114.4	exposure to various stages of a typical state of the art CAD VLSI tool be provided by various experiments	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C114.5	designed to bring out the key aspects of simulation, and power and clock routing modules.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C114.6	Know about the ASIC RTL realization of an available open source MCU	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C114.1	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C114.2	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C114.3	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C114.4	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C114.5	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C114.6	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C114	**1**	**1**	**1**	**1**	**1**	**3**	**3**	**3**	**2**	**2**	**2**	**2**	**2**	**2**	**1**

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C115- CP5281 TERM PAPER WRITING AND SEMINAR

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C115.1	develop their scientific and technical reading and writing skills that they need to understand and construct research articles	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.2	obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.3	Selection of area of interest and Topic	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.4	Stating an in writing Objective	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.5	Collecting Information about your area & topic	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C115.6	place it in logically developed ideas.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C115.1	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.2	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.3	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.4	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.5	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115.6	1	1	1	1	1	3	3	3	2	2	2	2	2	2	1
C115	**1**	**1**	**1**	**1**	**1**	**3**	**3**	**3**	**2**	**2**	**2**	**2**	**2**	**2**	**1**

SEM –III

C201- VL5301 Analog to Digital Interfaces

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C201.1	sampling the input analog signal for digitization and enabling circuit architectures .	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C201.2	Explain the principles of Analog to Digital conversion of signals.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C201.3	Explain the principles of Digital to Analog conversion of signals.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C201.4	Learn the importance of calibration techniques for achieving precision during data conversion	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C201.5	learn Switched capacitor circuits and comparators	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C201.6	learn comparators circuits	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C201.1	1	2	2	2	1	3	3	3	2	3	2	3	2	2	2
C201.2	1	2	2	2	1	3	3	3	2	3	2	3	2	2	2
C201.3	1	2	2	2	1	3	3	3	2	3	2	3	2	2	2
C201.4	1	2	2	2	1	3	3	3	2	3	2	3	2	2	2
C201.5	1	2	2	2	1	3	3	3	2	3	2	3	2	2	2
C201.6	1	2	2	2	1	3	3	3	2	3	2	3	2	2	2
C201	1	2	2	2	1	3	3	3	2	3	2	3	2	2	2

C202- AP5292 Digital Image Processing

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C202.1	Learn the fundamentals of digital images	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C202.2	Learn different image transforms	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C202.3	Explain the concept of segmentation	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C202.4	Discuss image enhancement techniques Explain color image processing Compare image compression schemes	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C202.5	Explain color image processing	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C202.6	Compare image compression schemes	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C202.1	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C202.2	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C202.3	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C202.4	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C202.5	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C202.6	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2
C202	2	2	2	2	2	2	3	3	3	3	3	3	2	2	2

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C203- VL5012 Selected Topics in IC Design

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C203.1	Explain the supply circuit modules which are crucial modules in an IC design.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C203.2	Learn about Clock generation circuits	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C203.3	Explain the High Speed Broad Band Communication circuits.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C203.4	High Speed I/O"s, Memory modules	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C203.5	High Speed Data Conversion Circuits.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C203.6	design aspect of Clock Generation circuits and their design constraints.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs,PSOs with POs

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C203.1	2	2	2	2	1	3	3	3	2	3	2	3	2	2
C203.2	2	2	2	2	1	3	3	3	2	3	2	3	2	2
C203.3	2	2	2	2	1	3	3	3	2	3	2	3	2	2
C203.4	2	2	2	2	1	3	3	3	2	3	2	3	2	2
C203.5	2	2	2	2	1	3	3	3	2	3	2	3	2	2
C203.6	2	2	2	2	1	3	3	3	2	3	2	3	2	2
C203	**2**	2	2	2	1	3	3	3	2	3	2	3	2	2

C204- VL5311 Project Work Phase-I

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C204.1	Identify challenging practical problems, solutions to cope up with present scenario of electronics field.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C204.2	. To collecting information related to the same through detailed review of literature	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C204.3	Analyze the various methodologies and technologies and discuss with the team for solving the problem	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C204.4	Apply technical knowledge and project management skills for solving the problem	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C204.5	Design and develop hardware and/or software for their project specific problem.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

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C204.6	Prepare the project reports and justify during presentation and demonstration	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C204.1	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C204.2	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C204.3	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C204.4	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C204.5	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C204.6	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C202	**1**	**1**	**1**	**1**	**1**	**3**	**1**	**3**	**3**	**3**	**2**	**2**	**1**	**1**	**1**

C205- VL5411 Project Work Phase-II

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C205.1	To solve the identified problem based on the formulated methodology	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.2	To develop skills to analyze and discuss the test results, and make conclusions	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.3	Apply technical knowledge and project management skills for solving the problem	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.4	On completion of the project work students will be in a position	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.5	To take up any challenging practical problem and find better solutions.	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3
C205.6	At the end of the course the students will have a clear idea of his/her area of work	1,2,3,4,5,6,7,8,9,10,11,12	1,2,3

Mapping of COs, PSOs with POs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
C205.1	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.2	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.3	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.4	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1

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C205.5	1	1	1	1	1	3	1	3	3	3	2	2	1	1	1
C205.6	**1**	**1**	**1**	**1**	**1**	**3**	**1**	**3**	**3**	**3**	**2**	**2**	**1**	**1**	**1**
C205	**1**	**1**	**1**	**1**	**1**	**3**	**1**	**3**	**3**	**3**	**2**	**2**	**1**		**1**

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