# Indra Ganesan
## COLLEGE OF ENGINEERING

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai
Accredited by NAAC with 'B+' Grade, 2(f) & 12B Status Institution by UGC
IG Valley, Madurai Main Road, Manikandam, Tiruchirappalli - 620012

# NAAC DOCUMENTS

## QUALITY INDICATOR FRAME WORK

## CRITERION – 1

## CURRICULAR ASPECTS

SUBMITTED BY

IQAC

INTERNAL QUALITY ASSURANCE CELL

INDRA GANESAN COLLEGE OF ENGINEERING

| Criteria 1 | Curricular Aspects | 100 |
|---|---|---|

## Curricular Planning and Implementation (20)

**The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment**

## Table of Content

# INDRA GANESAN COLLEGE OF ENGINEERING

**IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India**
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**DEPARTMENT OF ELCTRONICS AND COMMUNICATION ENGINEERING**

## PREFACE OF THE COURSE FILE

| | |
|---|---|
| Batch | : **2021-2023** |
| Academic Year | : **2022-2023 / ODD** |
| Program | : M.E VLSI DESIGN |
| Year & Semester | : **2nd Year / 3rd Semester / 'A' Section** |
| Course Code | : VL 4091 NBA Course Code: C202 |
| Name of the Course | : Network on Chip |
| Faculty in-charge | : Dr.M.Bhuvaneswari, Associate Professor / ECE |

Signature of the Faculty in-charge

HoD / ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
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# INDRA GANESAN COLLEGE OF ENGINEERING

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## Faculty Time Table

**Dr.M.Bhuvaneswari**

| Day Order | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| I | | VL4091 | | | | | | |
| II | | | | | | | | |
| III | | | | | | | | |
| IV | VL4091 | | | | | | VL4091 | |
| V | | | | VL4091 | | | | |

| S.Code | Title | Year / Branch | Hours |
|---|---|---|---|
| VL4091 | Network on Chip | II / M.E.VLSI DESIGN | 4 |
| | TOTAL - 4 hours | | |

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## DEPARTMENT OF ELCTRONICS AND COMMUNICATION ENGINEERING

### SYLLABUS

### VL4091 NETWORK ON CHIP

L T P C

3 0 0 3

**COURSE OBJECTIVES::**

The students should be made to:

- Understand the concept of Network - on - Chip
- Learn router architecture designs
- Study fault tolerance Network - on – Chip

**UNIT I INTRODUCTION TO NOC** 9

Introduction to NOC – OSI Layer Rules in NOC - Interconnection Networks in Network-On-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Qualityof-Service Support

**UNIT II ARCHITECTURE DESIGN** 9

Switching Techniques and Packet Format - Asynchronous FIFO Design - GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design

**UNITIII ROUTING ALGORITHM** 9

Packet Routing -QOS, Congestion Control and Flow Control – Router Design – Network Link Design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing For 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms – Reliable and Adaptive Routing Algorithms

**UNIT IV TEST AND FAULT TOLERANCE OF NOC** 9

Design-Security in Networks-On-Chips-Formal Verification of Communications in Networks-On Chips-Test and Fault Tolerance For Networks-On-Chip Infrastructures-Monitoring Services For Networks-On-Chips

**UNIT V THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP** 9

Three-Dimensional Networks-On-Chips Architectures – A Novel Dimensionally - Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation For QOS On-Chip Communication – Networks-On-Chip Protocols-On-Chip Processor Traffic Modeling For Networks On-Chip

**TOTAL:45 PERIODS**

**REFERENCES**

1. ChrysostoMOSnicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-On - Chip " Architectures Holistic Design Exploration", Springer.
2. Fayezgebali, Haythamelmiligi, Hqhahedwatheq E1-Kharashi "Networks-On-Chips Theory and Practice CRC Press
3. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-On-Chip Architectures" 2013
4. Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-On-Chip" 2014

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**Lecture Schedule**

Degree/Program: **B.E / ECE**
Duration: **Dec 2022 - March 2023**

Course code &Name: VL4091 - Network on Chip
Semester: III Section: A Faculty : Dr.M.Bhuvaneswari

**AIM:**

To study the concept of Network on Chip and Architecture design

**OBJECTIVES:**

The students should be made to:

(i) Explain the concept of Network - on - Chip

(ii) Learn router architecture designs

(iii) Study fault tolerance Network - on – Chip

**PREREQUISITES:** System on Chip , VLSI Design, Computer Networks

**COURSE OUTCOMES:**

After the course, the student should be able to:

| CO | Course Outcomes | POs | PSOs |
|---|---|---|---|
| C202.1 | Compare different architecture design | 1,2,3,4,5,6,7,8,9,10,11,12 | 1,2,3 |
| C202.2 | Discuss different routing algorithms | 1,2,3,4,5,6,7,8,9,10,11,12 | 1,2,3 |
| C202.3 | Explain three dimensional Networks on Chip architectures | 1,2,3,4,5,6,7,8,9,10,11,12 | 1,2,3 |
| C202.4 | Test and design fault tolerant NOC | 1,2,3,4,5,6,7,8,9,10,11,12 | 1,2,3 |
| C202.5 | Design three dimensional architectures of NOC | 1,2,3,4,5,6,7,8,9,10,11,12 | 1,2,3 |
| C202.6 | Study fault tolerance Network - on – Chip | 1,2,3,4,5,6,7,8,9,10,11,12 | 1,2,3 |

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| S.No | Date | Period | Topics to be Covered | Book & Page. No. |
|---|---|---|---|---|
| UNIT I - INTRODUCTION TO NOC | | | | Target periods :9 |
| 1 | 12.12.2022 | 2 | Introduction to NOC | R1 |
| 2 | 14.12.2022 | 7 | OSI Layer Rules in NOC | R1 |
| 3 | 15.12.2022 | 1 | Interconnection Networks in Network-On-Chip | R1 |
| 4 | 16.12.2022 | 4 | Interconnection Networks in Network-On-Chip | R1 |
| 5 | 19.12.2022 | 2 | Network Topologies | R1 |
| 6 | 21.12.2022 | 7 | Switching Techniques | R1 |
| 7 | 23.12.2022 | 4 | Routing Strategies | R1 |
| 8 | 26.12.2022 | 2 | Flow Control Protocol | R1 |
| 9 | 28.12.2022 | 7 | Quality of-Service Support | R1 |
| UNIT II - ARCHITECTURE DESIGN | | | | Target periods :9 |
| 10 | 30.12.2022 | 4 | Introduction | R1 |
| 11 | 02.01.2023 | 2 | Switching Techniques and Packet Format | R1 |
| 12 | 04.01.2023 | 7 | Asynchronous FIFO Design | R1 |
| 13 | 05.01.2023 | 1 | Asynchronous FIFO Design | R1 |
| 14 | 06.01.2023 | 4 | GALS Style of Communication | R1 |
| 15 | 09.01.2023 | 2 | Wormhole Router Architecture Design | R1 |
| 16 | 11.01.2023 | 7 | Wormhole Router Architecture Design | R1 |
| 17 | 12.01.2023 | 1 | VC Router Architecture Design | R1 |
| 18 | 18.01.2023 | 7 | Adaptive Router Architecture Design | R1 |
| UNIT III -ROUTING ALGORITHM | | | | Target Periods :9 |
| 19 | 19.01.2023 | 1 | Packet Routing-QOS | R4 |
| 20 | 20.01.2023 | 4 | Congestion Control and Flow Control | R4 |
| 21 | 23.01.2023 | 2 | Router Design | R4 |
| 22 | 25.01.2023 | 7 | Network Link Design | R4 |
| 23 | 02.02.2023 | 1 | Efficient and Deadlock | R4 |
| 24 | 03.02.2023 | 4 | Free Tree-Based Multicast Routing Methods | R4 |
| 25 | 06.02.2023 | 2 | Path-Based Multicast Routing For 2D and 3D Mesh Networks | R4 |
| 26 | 08.02.2023 | 7 | Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms | R4 |
| 27 | 09.02.2023 | 1 | | R4 |
| UNIT IV - TEST AND FAULT TOLERANCE OF NOC | | | | Target Periods :9 |
| 28 | 10.02.2023 | 4 | Introduction | R2 |
| 29 | 13.02.2023 | 2 | Design-Security in Networks-On-Chips | R2 |
| 30 | 15.02.2023 | 7 | Design-Security in Networks-On-Chips | |
| 31 | 16.02.2023 | 1 | Formal Verification of Communications in Networks-On Chips | R2 |
| 32 | 17.02.2023 | 4 | Test and Fault Tolerance For Networks-On-Chip Infrastructures | R2 |
| 33 | 20.02.2023 | 2 | Monitoring Services For Networks-On-Chips | R2 |
| 34 | 22.02.2023 | 7 | | |
| 35 | 23.02.2023 | 1 | | |
| 36 | 24.02.2023 | 4 | | |

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| | | | | |
|---|---|---|---|---|
| **UNIT V - THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP** | | | | **Target Periods:9** |
| 37 | 27.02.2023 | 2 | Three-Dimensional Networks-On-Chips Architectures | R3 |
| 38 | 01.03.2023 | 7 | Three-Dimensional Networks-On-Chips Architectures | R3 |
| 39 | 02.03.2023 | 1 | A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures | R3 |
| 40 | 03.03.2023 | 4 | A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures | R3 |
| 41 | 06.03.2023 | 2 | Resource Allocation For QOS On-Chip Communication | R2 & R3 |
| 42 | 08.03.2023 | 7 | Networks-On-Chip Protocols | R3 |
| 43 | 09.03.2023 | 1 | Networks-On-Chip Protocols | R3 |
| 44 | 10.03.2023 | 4 | On-Chip Processor Traffic Modeling For Networks On-Chip | R3 |
| 45 | 13.03.2023 | 2 | On-Chip Processor Traffic Modeling For Networks On-Chip | R3 |
| **Content Beyond the Syllabus** | | | | |
| 46 | 15.03.2023 | 7 | Wireless Network on Chip | Material |

**Book Reference – References**

| Sl.No | Title of the Book | Author | Publisher | Year |
|---|---|---|---|---|
| 1. | Networks-On - Chip " Architectures Holistic Design Exploration" | ChrysostoMOSnicopoulos, Vijaykrishnan Narayanan, Chita R.Das | Springer. | |
| 2. | Networks-On-Chips Theory and Practice | Fayezgebali, Haythamelmiligi, Hqhahedwatheq E1-Kharashi | CRC Press | |
| 3. | Designing 2D and 3D Network-On-Chip Architectures | Konstantinos Tatas and Kostas Siozios | | 2013 |
| 4 | Palesi, Maurizio, Daneshtalab, Masoud | Routing Algorithms in Networks-On-Chip | | 2014 |

**Website Reference:**

https://www.semanticscholar.org/reader/b09310d912dfd719f0f30fd1f72c58b1bfb053bb

Signature of the Faculty in-charge

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## Identification of Curricular Gap & Content Beyond Syllabus(CBS)

**Name of the Faculty :Dr.M.Bhuvaneswari** **Course Code & Name:VL4091 &Network on Chip**

**Degree & Program:B.E. /ECE** **Semester & Section: III / A** **Academic Year: 2021 -2022 /ODD**

**I.Mapping of Course Outcomes with POs & PSOs.( before CBS)**

**Table.1 Mapping of COs, C, PSOs with POs - before CBS.**

| Course | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C202.1 | 3 | 2 | 2 | 2 | 1 | - | - | - | 1 | 1 | 1 | 1 | 2 | 2 |
| C202.2 | 3 | 2 | 1 | 1 | - | - | - | - | - | 1 | - | 1 | 2 | 2 |
| C202.3 | 3 | 2 | 1 | 1 | - | - | - | - | - | - | - | - | 2 | 2 |
| C202.4 | 3 | 2 | 1 | 1 | - | - | - | - | - | - | - | - | 2 | 2 |
| C202.5 | 3 | 2 | 1 | 1 | - | - | - | - | - | - | - | - | 2 | 2 |
| C202.6 | 3 | 2 | 1 | 1 | - | - | - | - | - | - | - | - | 2 | 2 |
| C202 | 3 | 2 | 1 | 1 | - | - | - | - | - | - | - | - | 2 | 2 |

**II. Identification of content beyond syllabus.**

**Table.2 Identification of content beyond syllabus**

| Details of Content Beyond Syllabus(CBS) added | POs strengthened/ vacant filled | CO/Unit |
|---|---|---|
| Wireless Network on Chip | PO5(2) Vacant filled | C202.5 & C202.6/ IV & V |

**III. Mapping of Course Outcomes with POs & PSOs. (After CBS)**

**Table.3 Mapping of COs, C, PSOs with POs- after CBS.**

| Course | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C210.1 | 3 | 2 | 1 | 1 | - | - | - | - | - | - | - | - | 2 | 2 |
| C210.2 | 3 | 2 | 1 | 1 | - | - | - | - | - | - | - | - | 2 | 2 |
| C210.3 | 3 | 2 | 1 | 1 | - | - | - | - | - | - | - | - | 2 | 2 |
| C210.4 | 3 | 2 | 1 | 1 | - | - | - | - | - | - | - | - | 2 | 2 |
| C210.5 | 3 | 2 | 1 | 1 | *2 | - | - | - | - | - | - | - | 2 | 2 |
| C210.6 | 3 | 2 | 1 | 1 | *2 | - | - | - | - | - | - | - | 2 | 2 |
| C210 | 3 | 2 | 1 | 1 | *2 | - | - | - | - | - | - | - | 2 | 2 |

**Signature of the Faculty**

**HoD/ECE**

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## Identification of Curricular Gap & Content Beyond Syllabus(CBS)

**Name of the Faculty :Dr.M.Bhuvaneswari** **Course Code & Name:VL4091 &Network on Chip**

**Degree & Program:B.E. /ECE** **Semester & Section: III / A** **Academic Year: 2022 -2023 /ODD**

**MATERIAL**

### WIRELESS NETWORK ON CHIP

INTRODUCTION

Networks-on-Chip (NoCs) have emerged as communication backbones to enable a high degree of integration in multi-core Systems-on-Chip (SoCs). Despite their advantages, an important performance limitation in traditional NoCs arises from planar metal interconnect-based multi-hop communications, wherein the data transfer between two far apart blocks causes high latency and power consumption. There have been some efforts to address this problem by introducing ultra-low latency and low power express channels between highly separated nodes. Although these communication channels are significantly more efficient in terms of power and delay compared to their conventional counterparts, they are still metal wires. According to the International Technology Roadmap for Semiconductors (ITRS), improving characteristics of metal wires will no longer satisfy performance requirements and new interconnect paradigms are needed. Different approaches such as 3D, photonic NoCs and NoC architectures with multi-band RF interconnects have already been explored. All these approaches reduce the latency and power dissipation to some degree, but they do not generally solve the difficult problem of laying out interconnects across the chip.

WINOC ARCHITECTURE

The goal of on-chip communication system design is to transmit data with low latencies and high throughput using the least possible power and resources. Currently, the major challenges in traditional wire-based NoCs are the high latency and power consumption of their multi-hop links. A two-tier hybrid (wireless/wired) architecture to interconnect hundreds to thousands of cores in chip multiprocessors (CMPs) using wireless networking is proposed]. In the design of a wireless NoC based on CMOS ultra wideband (UWB) technology is demonstrated. An interrouter wireless scalable express channel for NoC architectures that reduces power consumption and area overhead and improves performance is proposed.. All these works predominantly use a regular wired mesh-based NoC overlaid with wireless links.

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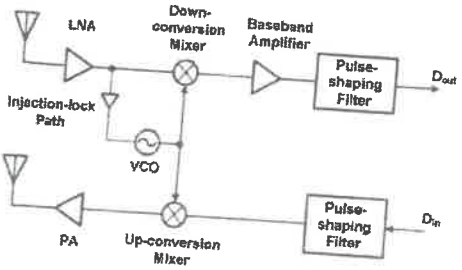
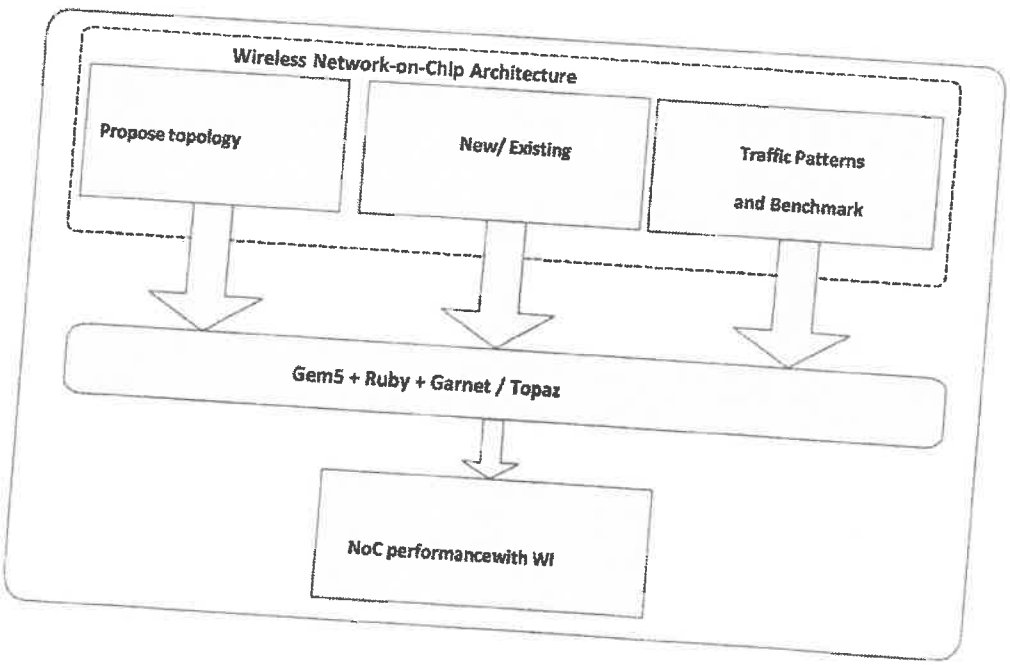
WIRELESS INTERFACE

Two principal components of the wireless interface (WI) are the antenna and the transceiver. According to the ITRS, the cut-off frequency and unity maximum available power gain frequency targets are 600 GHz and 1 THz respectively in 16 nm CMOS technology. With such scaling the required antenna and circuit areas will scale down. This allows easy on-chip integration. The on-chip antenna for the WiNoCs has to provide the best power gain for the smallest area overhead. A metal zig-zag antenna has been demonstrated to possess these characteristics and suits this application. This antenna also has negligible effect of rotation (relative angle between transmitting and receiving




Wireless interconnects operating in mm-wave range can provide efficient long range links inside a multi-core chip. But there is no simulator available that can directly simulate a NoC with wireless links. To prepare a wireless NoC simulator environment that provides a full system performance, a group of simulators viz. can be used . Gem5 is a cycle accurate full system simulator; Ruby is mainly used for network testing with synthetic traffic.

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Various design possibilities and challenges for wireless NoC (WiNoC) architectures as communication backbones for multi-core chips. We have highlighted several issues, including overall architecture, physical layer design, MAC protocols, routing, reliability and simulation setups. The WiNoC paradigm is still in its initial stages. It needs extensive investigations to make it a viable alternative to existing interconnect infrastructures.

**Signature of the Faculty**

**HoD/ECE**

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## Assignment Question Paper

| Assignment – 01 | | | Date of Issue: | 08.02.2023 | Marks | 10 |
|---|---|---|---|---|---|---|
| Course code | VL 4091 | Course Title | Network on Chip | | | |
| Year | II | Semester/Section | III /A | Date of Submission: | 22.02.2023 | |

| Q.No | Questions | CO |
|---|---|---|
| 1 | Explain Wormhole Router Architecture Design | C202.1 |
| 2 | Explain Adaptive Router Architecture Design | C202.2 |
| 3 | Discuss Design-Security in Networks-On-Chips | C202.4 |

M. Bhuvaneswari
[M. BHUVANESWARI]
**Name and Signature of the Faculty Incharge**

M. Bhuvaneswari
**HoD/ECE**

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## Assignment Answer Sheet

**Name of the Student : T. ABARNA**

**AU Register Number: 811221419001**

| Assignment – 01 | | | Date of Issue: | 08.02.2023 | Marks | 10 |
|---|---|---|---|---|---|---|
| Course code | VL 4091 | Course Title | Network on Chip | | | |
| Year | II | Semester/Section | III / A | Date of Submission: | 22.02.2023 | |

| Q.No | Questions | CO |
|---|---|---|
| 1 | Explain Wormhole Router Architecture Design | C202.1 |
| 2 | Explain Adaptive Router Architecture Design | C202.2 |
| 3 | Discuss Design-Security in Networks-On-Chips | C202.4 |

### Mark Allocation

| Rubrics | Marks Allocated | Marks obtained |
|---|---|---|
| Content Quality | 6 | 5 |
| Presentation Quality | 2 | 1 |
| Timely submission | 2 | 2 |
| Total marks | 10 | 8 |

M. Bhuvana

Name and Signature of the Faculty Incharge

M. Bhuvana

HoD/ECE

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Register Number:

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| Internal Assessment Exam - I | | | Date/Session | 20.01.2023 | Marks | 60 |
|---|---|---|---|---|---|---|
| Course code | VL4091 | Course Title | Network on Chip | | | |
| Regulation | 2021 | Duration | 90 minutes | Academic Year | 2022-23 | |
| Year | II | Semester | III | Department | M.E VLSI DESIGN | |

**COURSE OUTCOMES**

| | |
|---|---|
| C202.1 | Compare different architecture design |
| C202.2 | Discuss different routing algorithms |
| C202.3 | Explain three dimensional Networks on Chip architectures |
| C202.4 | Test and design fault tolerant NOC |
| C202.5 | Design three dimensional architectures of NOC |
| C202.6 | Study fault tolerance Network - on – Chip |

| Q.No. | Question | CO | BTS |
|---|---|---|---|
| | **PART A** (Answer all the Questions 10 x 2 = 20 Marks) | | |
| 1 | What is Network on Chip? | CO 1 | K1 |
| 2 | Compare Circuit switching and Packet Switching | CO 1 | K2 |
| 3 | Define Mesh Network | CO 1 | K1 |
| 4 | Define Quality of service | CO 1 | K2 |
| 5 | Define Flow control | CO 1 | K1 |
| 6 | What do you mean by Asynchronous FIFO design? | CO 2 | K2 |
| 7 | What do you mean by GALS Style of Communication | CO 2 | K2 |
| 8 | What is meant by Virtual channel router? | CO 2 | K2 |
| 9 | What do you mean by Wormhole routing? | CO 2 | K2 |
| | **PART B** (Answer all the Questions 2 x 14 = 28 Marks) | | |
| 10a | Explain OSI Layer Rules in NOC | CO 1 | K1 |
| | OR | | |
| 10b | Discuss Regular and Irregular topologies in On chip Network | CO 1 | K2 |
| 11a | Explain Asynchronous FIFO Design in NOC | CO 2 | K3 |
| | OR | | |
| 11b | Explain Wormhole router architecture design briefly in NOC | CO 2 | K2 |
| | **PART C** (Answer all the Questions 1 x 14 = 14 Marks) | | |
| 12a | Discuss Virtual Channel architecture design in NOC | CO 2 | K3 |
| | OR | | |
| 12b | Write Short notes on Flow control and Quality of support in NOC | CO 1 | K2 |

**Course Faculty**

**(Name /Sign / Date)**

**HoD**

**(Name /Sign / Date)**

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Internal Assessment Test Answer Book

| | | | | | |
|---|---|---|---|---|---|
| **Name** | T. ABARNA | | | **Year/ Semester/Section** | II / III Sem 'A' |
| **Batch No.** | 2021-23 | **Date/Session** | 20/01/2023 | **Department** | M.E. VLSI Design |
| **Course code** | VL4091 | **Course Title** | Network On Chip. | | |
| **Internal Assessment Test** | **IAT 1** ✓ ☐ | **IAT 2** ☐ | **IAT 3** ☐ | **Model** ☐ | |
| **Name and Signature of the Invigilator with date** | B.Lg 20/1/23 (B. SARASWATHI) | | | | |

Instruction to the Student: Put tick mark to the question attended in the column against question.

| Part A | | | Part B / Part C | | | | | | Total Marks |
|---|---|---|---|---|---|---|---|---|---|
| Q. No. | ✓ | Marks | Q. NO. | ✓ | a | ✓ | b | | |
| | | | | | Marks | | Marks | | |
| 1 | | 2 | 10 | | 12 | | | | 12 |
| 2 | | 2 | 11 | | 12 | | | | 12 |
| 3 | | — | 12 | | | | 12 | | 12 |
| 4 | | 2 | 14 | | | | | | |
| 5 | | 2 | 15 | | | | | | |
| 6 | | — | 16 | | | | | | |
| 7 | | 2 | | | | | Total | | 36 |
| 8 | | 2 | | | | | | | |
| 9 | | 2 | | | | | | | |
| 10 | | | | | | | | | |
| Total | | 14 | | | | | | | |

50/60

Grand Total

Name and Signature of the Examiner with date

**To be filled by the examiner**

| Course Outcomes | 1 | 2 | 3 | 4 | 5 | 6 | Total |
|---|---|---|---|---|---|---|---|
| Marks allotted | 30 | 20 | | | | | |
| Marks Obtained | 30 | 20 | | | | | |

**IQAC Audit - Remarks**

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

Name and Signature of the IQAC member

# INDRA GANESAN COLLEGE OF ENGINEERING

IG VALLEY, MANIDANDAM, TIRUCHIRAPPALLI – 620012

RTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2020 – 2021(EVEN SEMESTER)

**STUDENTS MARK STATEMENT- CO BASED**

INTERNAL ASSESSMENT TEST-I

SUBJECT CODE &TITLE: VL 4091 NETWORK ON CHIP

YEAR/SEM: II/ III MONTH & YEAR: JAN 2021

| S.NO | REG NO | STUDENT NAME | CO1 | CO2 | TOTAL (60) | TOTAL (100) |
|---|---|---|---|---|---|---|
| 1. | 811221419001 | T.ABARNA | 30 | 20 | 50 | 83 |
| 2. | 811221419003 | M.PREETHA | 13 | 12 | 25 | 42 |

MARKS RANGE:

| <20 | 20-30 | 31-40 | 41-50 | 51-60 | 61-70 | 71-80 | 81-90 | 91-100 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

| | |
|---|---|
| Total No.of Candidates Present | 2 |
| Total No.of Candidates Absent | 0 |
| Total No.of Students Pass | 1 |
| Total No. of Students Fail | 1 |
| Percentage of Pass | 50 % |

STAFF INCHARGE

HoD/ECE

PRINCIPAL

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

# INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India

(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### ROOT CAUSE ANALYSIS

**Name of the Faculty** : Dr. M. BHUVANESWARI
**Degree & Program** : M.E. VLSI Design
**IA Test** : I/II/III/Model
**Target** : 100 %

**Course Code & Name** : VL4091 & Network On Chip
**Semester & Section** : III Sem & A
**University Exam/Month & Year**: NOV/Dec 2022
**Achieved** : 50 %

| S.NO | BATCH NO | NAME OF THE STUDENT | CAUSES FOR FAILURE | SIGNATURE OF THE STUDENT WITH DATE | CORRECTIVE ACTION TAKEN | PREVENTIVE ACTION TAKEN | FOLLOWUP STATUS | REMARKS OF THE HOD |
|---|---|---|---|---|---|---|---|---|
| 1. | 811221419003 | Preetha. M. | Lack of Preparation | Preetha | Assignment Given. | Advised how to prepare, cover the unit | Progress monitored | Advised portion coverage is very important |

M. Bhuvaneswari

**Signature of the Faculty Member**

M. Bhuvaneswari

**Signature of the HoD/ ECE**

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

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## IQAC Academic Audit Form

ACADEMIC YEAR: 2022-23 SEMESTER 03

| Name of Department : | M.E VLSI Design | Year / Sem / Sec : | II / III A | No. of Students Registered : | 02 |
|---|---|---|---|---|---|
| Details of Examination : | IA Test -1 / IA Test -2 / IA Test -3 / Model Test | | | | |

| S.No. | Course Code | List of Reg.No Varified | Course Log Book Varified (Y / N) | Course File Varified (Y / N) | No of students Attended | No of Absentees | No of Failures | Pass % | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| 1. | VL4351 | 8112 21419001 | Y | Y | 2 | - | - | 100% | |
| 2 | VL4091 | 8112 21419001 | Y | Y | 2 | - | 1 | 50% | |
| 3 | DS415/ | 8112 21419003 | Y | Y | 2 | - | 1 | 50% | |
| 4 | OBA433 | 8112 21419003 | Y | Y | 1 | 1 | - | 50% | |
| | | | | | | | | | |
| | | | | | | | | | |

**Verified by**

| | |
|---|---|
| **External Member Name and Signature:** | Arun Pandiyan. S |
| **Internal Member Name and Signature:** | M. Nandhini & |

Overall Remarks:

Conduct Retest for failures.

HoD/ ECE

IQAC Co-ordinator

Principal

Dr. G. Balakrishnan, M.E., Ph.D.,
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.