Indra Ganesan
COLLEGE OF ENGINEERING

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai
Accredited by NAAC with 'B+' Grade, 2(f) & 12B Status Institution by UGC
IG Valley, Madurai Main Road, Manikandam, Tiruchirappalli - 620012

NAAC DOCUMENTS

QUALITY INDICATOR FRAME WORK

CRITERION – 1

CURRICULAR ASPECTS

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IQAC

INTERNAL QUALITY ASSURANCE CELL

INDRA GANESAN COLLEGE OF ENGINEERING

Criteria 1	Curricular Aspects	100

1.1 Curricular Planning and Implementation (20)

1.1.1 The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment

Table of Content

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PREFACE OF THE COURSE FILE

Batch	: 2021-2023
Academic Year	: 2021-2022 / EVEN
Program	: ELECTRONICS AND COMMUNICATION ENGINEERING
Year & Semester	: 1st Year / 2nd Semester
Course Code	: VL 4291
Name of the Course	: Low power VLSI design
Faculty in-charge	: P. Santhana Selvi AP/ECE

Signature of the Faculty in-charge

M. Bhuvaneswari
HoD / ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

Indra Ganesan
COLLEGE OF ENGINEERING

Madurai Main Road (NH-45B), Manikandam, Tiruchirappalli - 620 012

Department of Electronics and Communication Engineering

Academic Year 2021-22 **w.e.f: 26.07.2**

I-yr/-II Sem M.E (VLSI DESIGN) **CC: Mrs.M.Bhuvaneswari**

DAY	Test 9.15-10.00	1 10.00-10.45	BREAK	2 11.00-11.45	3 11.45-12.30	4 12.30-1.15	LUNCH	5 2.00-2.45	6 2.45-3.15	BREAK	7 3.30-4.15	8 4.15-5.00
MON	LP	VLSI TESTIN		DM	EMIC	LP		LIB	SEMINAR		RFIC	LP
TUE	SOC	EMIC		LIB	UVM	RFIC		VLSI TESTING	SOC		DM	SEMINAR
WED	RFIC	LP		EMIC	RFIC	UVM LAB		UVM LAB			UVM LAB	DM
THU	UVM	SOC		VLSI TESTIN	LP	SOC		UVM	EMIC		SOC	LIB
FRI	EMIC	UVM		RFIC	RESEARCH PAPER WRITING			VLSI TESTING	LP		UVM	COUNSELLING

SUBJECT CODE	COURSE NAME	ERP ID	CREDIT S/	STAFF IN-CHARGE
II4092	System on Chip		3 4	Mrs.M.Bhuvaneswari AOP ECE
VL4291	Low Power VLSI Design		3 4	Mrs.P.Santhana selvi AP ECE
VL4251	Design for Verification using UVM		3 4	Mrs.D.Kokila AP ECE
VL4252	VLSI Testing		3 4	Dr.S.Vasnatha swaminathan & Mrs.Nandhini AP ECE
VL4292	RFIC Design		3 4	Mrs.B.Saraswathi AP ECE
EL4071	Electromagnetic Interference and Compatibility		3 4	Mrs P.Jency Leena AP ECE
AX4092	Distaster Management		2 3	Mrs.N.Ramya HoD ECE
VL4212	Term Paper and Seminar		2/2	Mrs.M.Bhuvaneswari/AOP/ECE
VL4211	Verification using UVM Laboratory		2/4	Mrs.D.Kokila AP/ECE & S.Vasnatha Swaminathan
	Library /Seminar /Counselling		5	Mrs.G.Keerthana AP ECE

Timetable Coordinator HoD /ECE Principal

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

VL4291 **LOW POWER VLSI DESIGN** L T P C
3 0 0 3

COURSE OBJECTIVES:

- identify sources of power in an IC.
- identify the power reduction techniques based on technology independent and technology dependent methods
- identify suitable techniques to reduce the power dissipation
- estimate power dissipation of various MOS logic circuits
- develop algorithms for low power dissipation

UNIT I POWER DISSIPATION IN CMOS 9

Hierarchy of Limits of Power – Sources of Power Consumption – Physics of Power Dissipation in CMOS FET Devices – Basic Principle of Low Power Design.

UNIT II POWER OPTIMIZATION 9

Logic Level Power Optimization – Circuit Level Low Power Design – Gate Level Low Power Design –Architecture Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, PLL, Low Power Design

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer Arithmetic Techniques for Low Power System – Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories – Low Power Clock – Advanced Techniques – Special Techniques, Adiabatic Techniques – Physical Design, Floor Planning, Placement and Routing.

UNIT IV POWER ESTIMATION 9

Power Estimation Techniques, Circuit Level, Gate Level, Architecture Level, Behavioral Level, – Logic Power Estimation – Simulation Power Analysis –Probabilistic Power Analysis

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

UNIT V **SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER CMOS CIRCUITS** **9**

Synthesis for Low Power – Behavioral Level Transform –Algorithms for Low Power – Software Design for Low Power.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students should will be able to:

CO1: able to find the power dissipation of MOS circuits
CO2: design and analyze various MOS logic circuits
CO3 :apply low power techniques for low power dissipation
CO4: able to estimate the power dissipation of ICs
CO5: able to develop algorithms to reduce power dissipation by software.

REFERENCES

1. Kaushik Roy and S.C.Prasad, "Low Power CMOS VLSI Circuit Design", Wiley, 2000
2. J.B.Kulo and J.H Lou, "Low Voltage CMOS VLSI Circuits", Wiley 1999.
3. James B.Kulo, Shih-Chia Lin, "Low Voltage SOI CMOS VLSI Devices and Circuits", John Wiley and Sons, Inc. 2001
4. J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems)", Springer, 2009

CO-PO Mapping

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	2	0	2	3	3	0
2	2	0	2	2	3	0
3	1	0	2	2	3	0
4	1	0	2	3	2	0
5	2	0	2	2	1	0
Avg	(8/5)=1.6	(0/0)=0	(10/5)=2	(12/5)=2.4	(12/5)=2.4	(0/0)=0

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Ro
Manikandam, Trichy-6

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Faculty Time Table

Mrs.P.Santhana selvi

Day Order	1	2	3	4	5	6	7	8
I				VL4291				VL4291
II								
III	VL4291							
IV			VL4291					
V						VL4291		

S.Code	Title	Year / Branch	Hours
VL4291	Low Power VLSI Design	I/M.E VLSI DESIGN	5
TOTAL - 5 hours			

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
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IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Lecture Schedule

Degree/Program: **M.E / VLSI DESIGN** Course code &Name: **VL4291**–LOW POWER VLSI DESIGN
Duration: **June 2022 – Oct 2022** Semester: **II** Section: **A** Faculty: P.Santhana Selvi

AIM:

To teach the students about the analysis of low power system design

OBJECTIVES:

To impart knowledge on

(i) Identify sources of power in an IC
(ii) Identify the power reduction techniques based on technology independent and technology dependent methods
(iii) Identify suitable techniques to reduce the power dissipation
(iv) Estimate power dissipation of various MOS logic circuits
(v) Develop algorithms for low power dissipation
(vi) To design chips used for battery-powered systems and high performance circuits

PREREQUISITES:

Analog IC Design

COURSE OUTCOMES:

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C110.1	Able to find the power dissipation of MOS circuits	2,0,2,3,3,0	3
C110.2	Design and analyze various MOS logic circuits	2,0,2,2,3,0	2
C110.3	Apply low power techniques for low power dissipation	1,0,2,2,3,0	2
C110.4	Able to estimate the power dissipation of ICs	1,0,2,3,2,0	2
C110.5	Able to develop algorithms to reduce power dissipation by software	2,0,2,2,1,0	2

S.No	Date	Period	Topics to be Covered	Book & Page. No.
UNIT -I - POWER DISSIPATION IN CMOS				**Target periods :9**
1	27/06/22	4	Hierarchy of Limits of Power	R1
2	27/06/22	8	Hierarchy of Limits of Power Contd	R1
3	29/06/22	1	Sources of Power Consumption	R2
4	30/06/22	3	Sources of Power Consumption - Contd	R1
5	01/07/22	6	Physics of Power Dissipation in CMOS FET Devices – Basic Principle of Low Power Design.	R1

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
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6	02/07/22	3	Physics of Power Dissipation in CMOS FET Devices – Basic Principle of Low Power Design.	R1
7	04/07/22	4	Physics of Power Dissipation in CMOS FET Devices -contd	R1,R2
8	04/07/22	8	Basic Principle of Low Power Design	R1
9	06/07/22	1	Problems	R1
UNIT II - POWER OPTIMIZATION				**Target Periods :9**
10	07/07/22	3	Logic Level Power Optimization	R2,R1
11	08/07/22	6	Circuit Level Low Power Design	R3,R1
12	11/07/22	4	Gate Level Low Power Design	R1
13	11/07/22	8	Architecture Level Low Power Design	R2,R1
14	13/07/22	1	VLSI Subsystem Design of Adders	R2,R1
15	14/07/22	3	VLSI Subsystem Design of Multipliers	R1,R1
16	15/07/22	6	VLSI Subsystem Design of PLL	R2,R1
17	18/07/22	4	VLSI Subsystem Design of Low Power Design	R1
18	18/07/22	8	Problems	R1
UNIT III - DESIGN OF LOW POWER CMOS CIRCUITS				**Target Periods :9**
19	20/07/22	1	Computer Arithmetic Techniques for Low Power System	R2,R1
20	21/07/22	3	Reducing Power Consumption in Combinational Logic	R3,R1
21	22/07/22	6	Reducing Power Consumption in Sequential Logic	R1
22	25/07/22	4	Reducing Power Consumption in Memories	R2,R1
23	25/07/22	8	Low Power Clock	R2,R1
24	27/07/22	1	Advanced Techniques – Special Techniques, Adiabatic Techniques	R1,R1
25	28/07/22	3	Physical Design, Floor Planning	R2,R1
26	29/07/22	6	Placement and Routing.	R1
27	01/08/22	4	Problems	R1
UNIT IV - POWER ESTIMATION				**Target Periods :9**
28	03/08/22	1	Power Estimation Techniques, Circuit Level	R2
29	04/08/22	3	Power Estimation Techniques, Gate Level	R3,R4
30	17/08/22	1	Power Estimation Techniques, Architecture Level	R4
31	18/08/22	3	Power Estimation Techniques, Behavioral Level	R2,R1
32	22/08/22	4	Logic Power Estimation	R3,R1
33	25/08/22	3	Logic Power Estimation-Contd	R1,R1
34	26/08/22	6	Simulation Power Analysis	R4,R1
35	29/08/22	4	Probabilistic Power Analysis	R1
36	01/09/22	3	Problems	R2
UNIT V - SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER CMOS CIRCUITS Target Periods:9				
37	02/09/22	6	Synthesis for Low Power	R2,R1
38	05/09/22	4	Synthesis for Low Power=Contd	R3,R1
39	07/09/22	1	Behavioral Level Transform	R1
40	08/09/22	3	Behavioral Level Transform-Contd	R2,R1
41	09/09/22	6	Algorithms for Low Power	R2,R1

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

42	12/09/22	4	Algorithms for Low Power-Contd	R4
43	14/09/22	1	Software Design for Low Power	R4
44	15/09/22	3	Software Design for Low Power -Contd	R2
45	16/09/22	6	Problems	R1,R2
Content Beyond the Syllabus				
46	17/09/22	1	Implementing Low Power Design Through Voltage Scaling in VLSI	Material

Book Reference- References

Sl	Title of the Book	Author	Publisher	Year
1.	Low Power CMOS VLSI Circuit Design	Kaushik Roy and S.C.Prasad	Wiley	2000
2.	Low Voltage CMOS VLSI Circuits	J.B.Kulo and J.H Lou	Wiley	1999
3.	Low Voltage SOI CMOS VLSI Devices and Circuits	James B.Kulo, Shih-Chia Lin	John Wiley and Sons	2001
4.	Low Power Design Essentials (Integrated Circuits and Systems)	J.Rabaey	Springer	2009

Website References:

1.https://onlinecoursin/noc22_ee55
2. https://archive.nptel.ac.in/courses/106/105/106105034/

Signature of the Faculty in-charge

HoD / ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Identification of Curricular Gap & Content Beyond Syllabus(CBS)

Name of the Faculty :Mrs.P..Santhana Selvi **Course Code & Name:** VL4291 Low power VLSI design

Degree & Program: M.E /VLSI DESIGN **Semester & Section: II / A** **Academic Year: 2021 -2022/EVEN**

I. Mapping of Course Outcomes with POs & PSOs.(before CBS)

Table.1 Mapping of COs, C, PSOs with POs – before CBS.

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C110.1	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C110.2	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C110.3	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C110.4	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C110.5	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C110.6	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C110	**1**	**1**	**1**	**1**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**1**	**1**

II. Identification of content beyond syllabus.

Table.2 Identification of content beyond syllabus

Details of Content Beyond Syllabus(CBS) added	POs strengthened/ vacant filled	CO/Unit
Implementing Low Power Design Through Voltage Scaling in VLSI	PO4 strenghened	C110.3/ III

III. Mapping of Course Outcomes with POs & PSOs. (After CBS)

Table.3 Mapping of COs, C, PSOs with POs- after CBS.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C110.1	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C110.2	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C110.3	1	1	1	*2	2	3	3	3	3	3	3	3	1	1	1
C110.4	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C110.5	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C110.6	1	1	1	1	2	3	3	3	3	3	3	3	1	1	1
C110	**1**	**1**	**1**	**1**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**1**	**1**

Signature of the Faculty

HoD/ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
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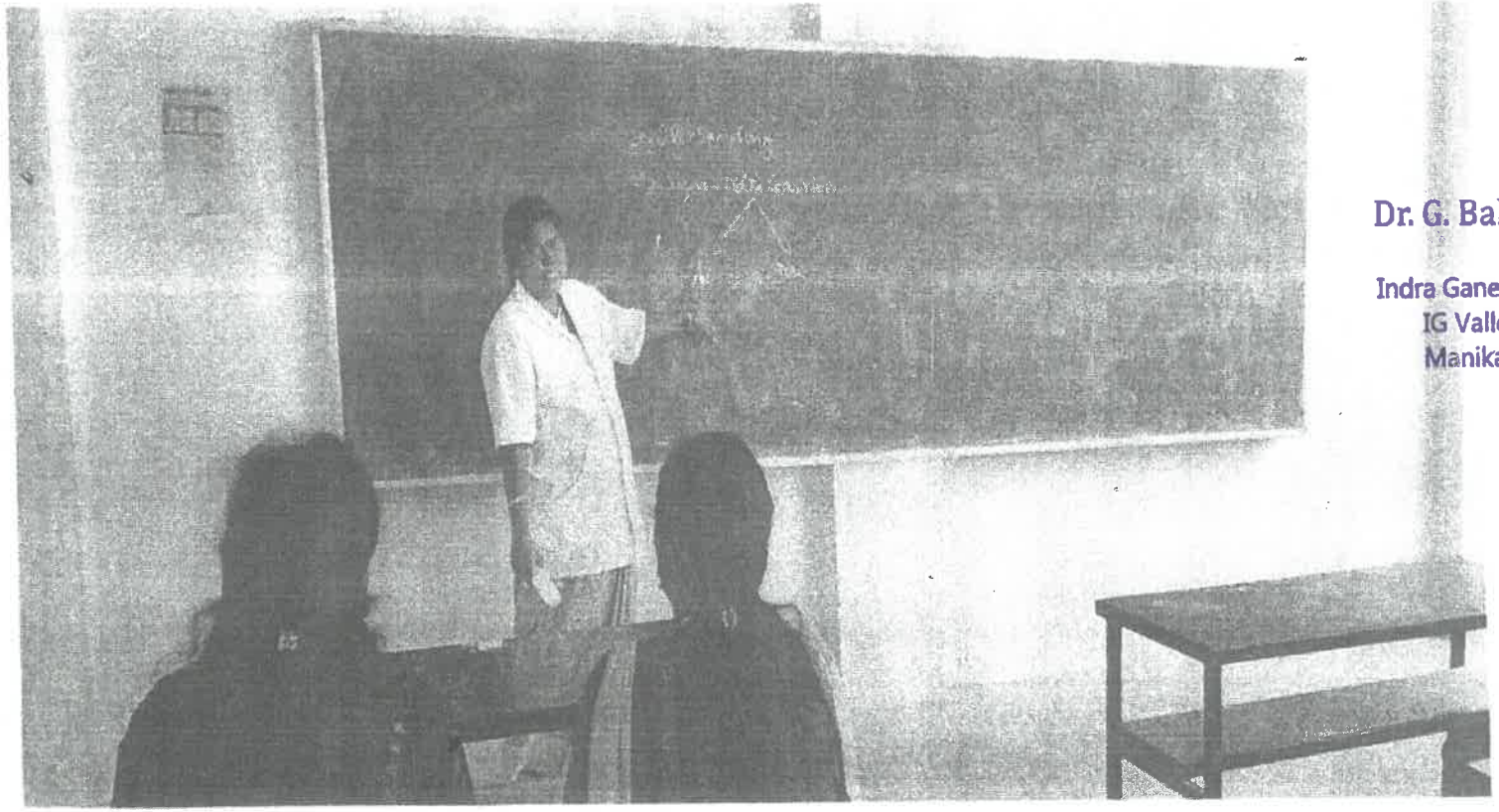
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Proof of Curricular Gap & Content Beyond Syllabus(CBS)

Name of the Faculty :Mrs.P.Santhanaselvi Course Code & Name:VL4291-Low Power VLSI Design Degree & Program:M.E. /VLSI Design Semester & Section: II / A Academic Year: 2021 -2020 /EVEN



Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

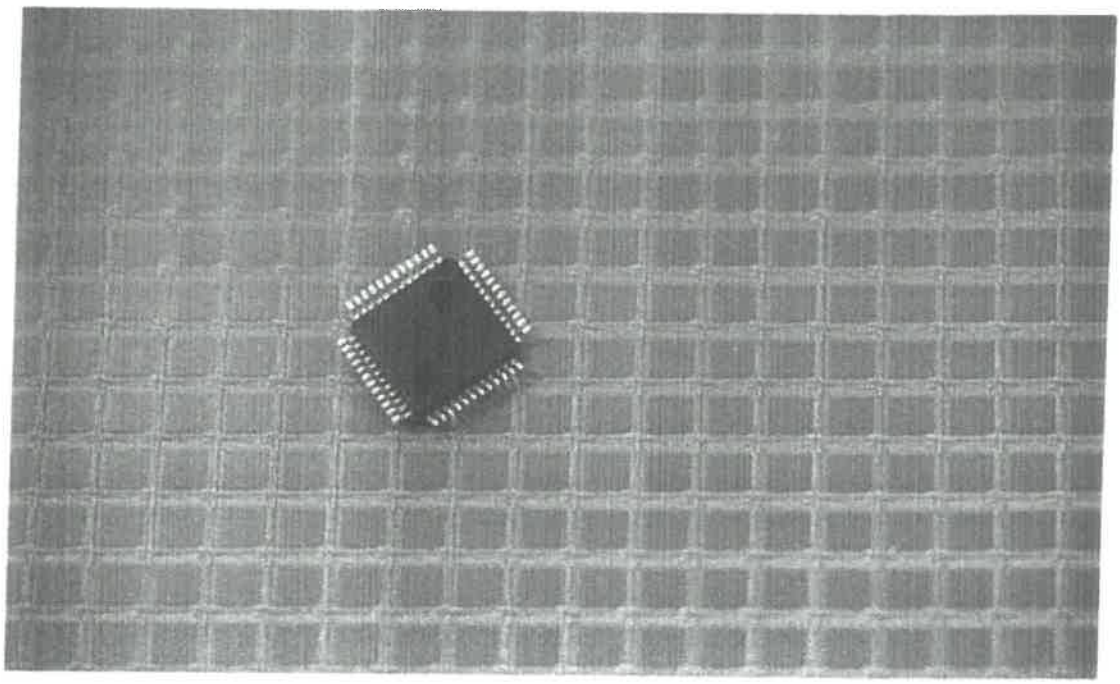
Signature of the Faculty

HoD/ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

Implementing Low Power Design Through Voltage Scaling in VLSI

- The dominant integrated circuit (IC) design paradigm is very large scale integration (VLSI).
- . Newer, more advanced CMOS products have more features integrated on-die than in the past, and these features can consume more power at higher clock rates.
- Low power design through voltage scaling is one simple method to turn features on and off using logic circuits builtinto the component.



Deep within the chips on this wafer are regulation and managementcircuits for lower power operation

While you can't easily crack open the case of an integrated circuit (IC) to see its features, rest assured that today's advanced products are nothing like their predecessors from over two decades ago.Today's chips pack many features into a small die with unique circuit architectures that help ensure power-efficient data transfer inside and outside the component. Moore's Law has driven the size of transistors and logic circuits smaller. But, it has also moved feature density and power consumption higher, forcing designers to get creative and come up with power management strategies.

Although core voltages have lowered, especially in some very high- speed systems like large FPGAs, power management strategies are implemented to control switching thresholds and logic levels. These strategies are implemented with voltage scaling in VLSI. Low power design through voltage scaling

strategies can be implemented readily throughout logic blocks alongside other low-power design strategies using some simple architectures.

Low Power Design Through Voltage Scaling

Voltage scaling involves adjusting the supply voltage (VDD) and the threshold voltage (VT) for logic levels in CMOS logic circuits to control the total power dissipation in a logic block. Buffer and logic circuits can be controlled in groups, allowing features to be switched on and off or dynamically adjusted as the chip operates.
This process can be done without modifying the system or peripheral clocks, so the system still maintains high speed even if the logic/supply levels are reduced.

Implementation

Low power design through voltage scaling is implemented with a specialty logic control circuit. The logic control circuit implementsvoltage scaling in two areas:

- Substrate bias control: This controls the threshold that defines digital states in logic circuits. A voltage is applied to the substrate regions in CMOS buffers to increase or decrease the threshold voltage and reduce leakage current when the device is placed on standby. This technique is sometimes called "back biasing."
- Supply (VDD) voltage control: This defines core logic levels in the design and requires adjusting the regulator circuit that sets supply voltages. The power delivered to a MOSFET circuit is proportional to the square of the supply voltage, so small changes in supply voltage can produce a proportionally large change in power delivery.

An example topology used to implement low power design through voltage scaling in CMOS logic circuits is shown below:

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

However, this also allows more current to flow during switching as the MOSFET capacitances charge up, which increases the average current during a given clock cycle.

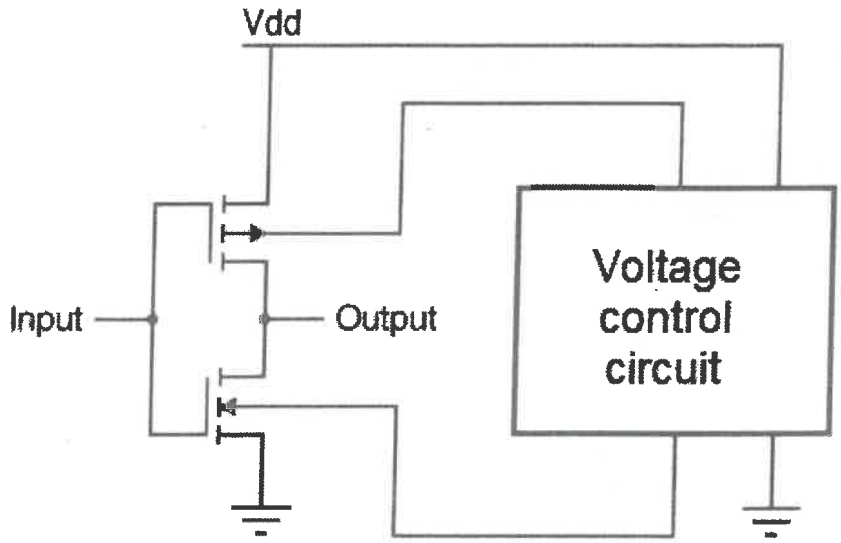
Low Power Design With Clock Control

While dynamic voltage scaling is a standard feature implemented in VLSI design, it isn't the only method used to build low-power systems. In addition to voltage scaling, modern VLSI designs implement clock control features to adjust total power consumption. The two methods used for clock control are:

- Clock gating: The most straightforward way to eliminate power consumption in a logic block while maintaining the states in logic circuits is to cut off the system clock from certain logic blocks. This method eliminates dynamic power consumption due to switching, leaving leakage as the primary power dissipation mechanism in these blocks.
- Dynamic frequency scaling: The power dissipated by logic circuits is proportional to the clock frequency. Therefore, the clock frequency can be ramped up or down as needed using an internal logic control circuit, VCO/NCO, and PLL. This option can be applied to the system clock or peripheral clocks.

Voltage scaling, frequency scaling, and clock gating are generally implemented together on modern chips, so systems designers have complete control over power consumption in their designs. The challenge in developing these systems is determining the appropriate regulatory strategy to implement on-chip versus which features developers should implement in firmware. Modern VLSI designs should allow developers to implement any strategy alongside the typical standby functions found in modern ICs.
These active scaling mechanisms don't necessarily require modifying the structure of transistors in logic circuits. They can be implemented in a new product with the best VLSI systems design and analysis tools.
When you need to implement low power design through voltage scaling, unique transistor architectures, or other power management strategies, use the complete set of system analysis tools from Cadence to qualify your designs. Only Cadence offers a comprehensive set of the circuit, IC, and PCB design tools for any application and any level of complexity.

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.



Even after implementing low power design techniques, this GPU will dissipate a significant amount of heat

In this topology, the control circuit must be custom designed so voltages can be adjusted under specific logical conditions. The required logical conditions will be different for every system, and they could be triggered by the system's firmware if needed in thedesign.

Advantages and Disadvantages

The use of voltage scaling provides two particular benefits in VLSI designs. First, it offers flexible scaling of logic levels (supply voltage) on-demand to control power consumption in the design. Second, it allows the standby leakage current to be controlled if circuit blocks are switched off, which is accomplished by adjusting the threshold voltage (body bias level). Controlling both voltages ensures lower power consumption during switching and standby.

The major disadvantage of low power design through voltage scaling is the increased propagation delay in logic circuits. Power dissipation and propagation delay are inversely related because ofthe nonlinear capacitance present in MOSFETs. By increasing the supply and substrate bias voltages, the applied capacitance increases, decreasing the switching time between logic states.

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Assignment Question Paper

Assignment – 01			Date of Issue:	20/07/2022	Marks	10
Course code	VL4291	Course Title	Low power vlsi design			
Year	I	Semester/Section	II/ A	Date of Submission:	29/07/2022	

Q.No	Questions	CO
1	What is the need for power reduction?	C110.1
2	Why low power has become an important issue in the present day VLSI circuit realization?	C110.1
3	Explain the various capacitances present in MOS and their effect on power dissipation with necessary diagrams and expressions	C110.1
4	Explain the principles and challenges in low power design	C110.1

R. Sarthanaselvi & A. Sivanmani
Name and Signature of the Faculty Incharge

M. Bhuvaneswari
HoD/ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Assignment Answer Sheet

Name of the Student : Abarna T

AU Register Number: 811221419001

Assignment – 01			Date of Issue:	20/07/2022	Marks	10
Course code	VL4292	Course Title	Low power vlsi design			
Year	I	Semester/Section	II A	Date of Submission:	29/07/2022	

Q.No	Questions	CO
1	What is the need for power reduction?	C110.1
2	Why low power has become an important issue in the present day VLSI circuit realization?	C110.1
3	Explain the various capacitances present in MOS and their effect on power dissipation with necessary diagrams and expressions	C110.1
4	Explain the principles and challenges in low power design	C110.1

Mark Allocation

Rubrics	Marks Allocated	Marks obtained
Content Quality	6	5
Presentation Quality	2	1
Timely submission	2	2
Total marks	10	8

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

P. Santhanaselvi & P. Sam
Name and Signature of the Faculty Incharge

H. Bhuvaneswari
HoD/ECE

Register Number: | | | | | | | | | | | |

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India

(Approved by AICTE, New Delhi and affiliated to Anna University, Chennai)

Internal Assessment Exam - I			Date/Session	08/08/2022/FN	Marks	60
Course code	VL4291	Course Title	Low power vlsi design			
Regulation	2021	Duration	90 minutes	Academic Year	2021-2022	
Year	I	Semester	III	Department	M.E/VLSI DESIGN	

COURSE OUTCOMES

C110.1	Able to find the power dissipation of MOS circuits
C110.2	Design and analyze various MOS logic circuits
C110.3	Apply low power techniques for low power dissipation
C110.4	Able to estimate the power dissipation of ICs
C110.5	Able to develop algorithms to reduce power dissipation by software
C110.6	Design chips used for battery-powered systems and high performance circuits

Q.No.	Question	CO	BTS
	PART A (Answer all the Questions 9 x 2 = 18 Marks)		
1	What is need for low power in VLSI design?	CO1	K1
2	State the effect of LDD structure in CMOS design?	CO1	K1
3	Name three sources of power dissipation in CMOS digital circuits	CO1	K1
4	How environment is affected by the power dissipation of VLSI circuits?	CO1	K2
5	What is body effect? How does it influences the threshold voltage of a MOS transistor?	CO1	K1
6	What is signal gating?	CO2	K1
7	Explain how parallelism can be used to achieve low power instead of high performance in realizing digital circuits	CO2	K2
8	What are the various reduce ways to the delay time of a CMOS inverter?	CO2	K1
9	What is logic level optimization?	CO2	K1
	PART B (Answer all the Questions 2 x 14 = 28 Marks)		
10a	Draw the energy band structure of MIS diode under unbiased and bias condition and discuss the various factors influencing power dissipation	CO1	K1
	OR		
10b	Explain in detail the physics of power dissipation in submicron MOSFET	CO1	K1
11a	Discuss in detail any four limits for low power design	CO1	K2
	OR		
11b	For CMOS inverter ,determine the expression for static power dissipation and dynamic power dissipation	CO1	K2
	PART C (Answer all the Questions 1 x 14 = 14 Marks)		
12a	Explain the optimization techniques for combinational circuits	CO2	K2
	OR		
12b	With example explain the importance of transistor sizing in power dissipation	CO2	K2

Course Faculty

(Name /Sign / Date)

P. SANTHIYA SELVI

HoD

(Name /Sign / Date)

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

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INDRA GANESAN COLLEGE OF ENGINEERING

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Internal Assessment Exam - I			Date/Session	08/08/2022/FN	Marks	60
Course code	VL4291	Course Title	Low power vlsi design			
Regulation	2021	Duration	90 minutes	Academic Year	2021-2022	
Year	I	Semester	III	Department	M.E/VLSI DESIGN	

COURSE OUTCOMES

C110.1	Able to find the power dissipation of MOS circuits
C110.2	Design and analyze various MOS logic circuits
C110.3	Apply low power techniques for low power dissipation
C110.4	Able to estimate the power dissipation of ICs
C110.5	Able to develop algorithms to reduce power dissipation by software
C110.6	Design chips used for battery-powered systems and high performance circuits

Answer Key

Q.No.	Question	CO	BT
	PART A (Answer all the Questions 9 x 2 = 20 Marks)		
1	What is need for low power in VLSI design? The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. This article reviews various strategies and methodologies for designing low power circuits and systems. It describes the many issues facing designers at architectural, logic, circuit and device levels and presents some of the techniques that have been proposed to overcome these difficulties.	CO1	K1
2	State the effect of LDD structure in CMOS design? As the LDD structure exhibits higher series parasitic resistance, an optimum supply voltage again exists. For larger values of supply voltage the delay increases. The occurrence of velocity saturation in submicromerter devices makes delay relatively independent of supply voltage. Hence for not too large delay penalty, reducing the supply voltage can reduce power dissipation	CO1	K1
3	Name three sources of power dissipation in CMOS digital circuits Logic transition-As the nodes in a digital CMOS circuit transition back and forth between the two logic levels,the parasitic capacitances are charged and discharged ii. As the voltage swing is equal to the supply voltage,the dissipation due to transitions varies overall as the square of the supply voltage.Short circuit current that flow directly from supply to ground when the n-subnetwork and p- subnetwork of a CMOS gate both conduct simultaneously iii. It is the leakage current that flows when the input to,and therefore the outputs of a gate are not changing	CO1	K1
4	How environment is affected by the power dissipation of VLSI circuits? According to an estimate of the U.S. Environmental Protection Agency (EPA), 80% of the power consumption by office equipment are due to computing equipment and a large part from unused equipment. Moreover, the power is dissipated mostly in the form of heat. The cooling techniques, such as AC transfers the heat to the environment	CO1	K2
5	What is body effect? How does it influences the threshold voltage of a MOS transistor? All MOS transistors are usually fabricated on a common substrate and substrate (body) voltage of all devices is normally constant. However, as we shall see in subsequent chapters, when circuits are realized using a number of MOS devices, several devices are connected in series. This results in different source potentials for different devices. It may be noted that	CO1	K1

	the threshold voltage Vt is not constant with respect to the voltage difference between the substrate and the source of the MOS transistor. This is known as the substrate-bias effect or *body effect*. Increasing the Vsb causes the channel to be depleted of charge carries and this leads to increase in the threshold voltage.		
6	What is signal gating? A data driven approach to design and optimization of low power combinational multipliers is presented. This technique depends on signal gating to avoid un-necessary computations and thus reduce the switching activity and power consumption of combinational multipliers. The proposed technique can be equally well applied to signed and unsigned multiplications. At the same time, it imposes reasonable area and delay overhead on the circuit. The benchmark data is extracted from typical DSP applications to show the efficiency of the proposed technique in the domain of DSP computations in which the low power computing is of rapidly increasing importance. The results show an average of 26% percent reduction in the switching activity and 22% area and 27% delay overhead, compared to combinational multipliers without this technique	CO2	K1
7	Explain how parallelism can be used to achieve low power instead of high performance in realizing digital circuits Traditionally, parallelism is used to improve performance at the expense of larger power dissipation. But, instead of trying to improve performance, the power dissipation can be reduced by scaling down the supply voltage such that the performance remains unaltered	CO2	K2
8	What are the various reduce ways to the delay time of a CMOS inverter? Various ways for reducing the delay time are given below: (a) The width of the MOS transistors can be increased to reduce the delay. This is known as gate sizing (b) The load capacitance can be reduced to reduce delay. This is achieved by using transistors of smaller and smaller dimensions as provided by future generation technologies. (c) Delay can also be reduced by increasing the supply voltage V_{dd} and/or reducing the threshold voltage V_t of the MOS transistors	CO2	K1
9	What is logic level optimization? The power optimization of a logic circuit implies the reduction of its switching activity of switched capacitance	CO2	K1

PART B

(Answer all the Questions 2 x 10 = 20 Marks)

10a	Draw the energy band structure of MIS diode under unbiased and bias condition and discuss the various factors influencing power dissipation	CO1	K1

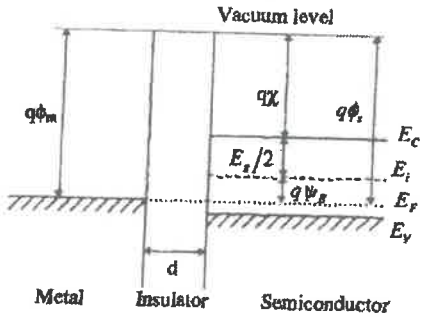
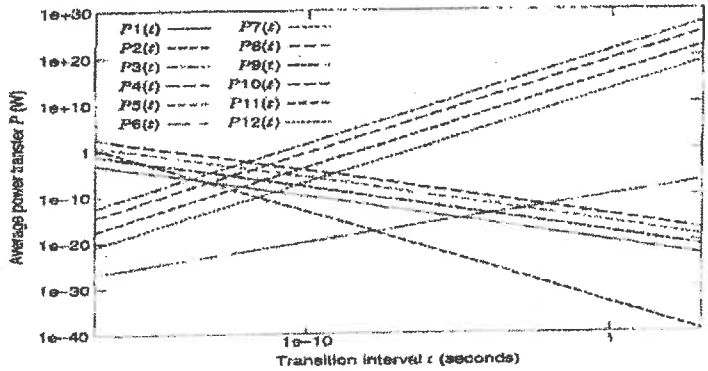


Figure 2.2 Energy bands in an unbiased MIS diode.

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

The MIS Structure

When the voltage V is negative, the holes in the p-type semiconductor are attracted to and accumulate at the semiconductor surface in contact with the insulator layer. Therefore this condition is called *accumulation*. In the absence of a current flow, the carriers in the semiconductor are in a state of equilibrium and the Fermi level appears as a straight line. The Maxwell–Boltzmann statistics relates the equilibrium hole concentration to the intrinsic Fermi level:

	OR		
10b	Explain in detail the physics of power dissipation in submicron MOSFET A recent model, according to Liu et al. predicts the short-channel threshold voltage shift $\Delta V_{T,sc}$ accurately even for devices with channel length below 0.5 μm [7]. Liu et al. adopt a quasi two-dimensional approach to solving the two-dimensional Poisson equation. The electric field vector **E** is regarded as having a horizontal component E_y and a vertical component E_x. The term E_y is the drain field. The drain field has only a horizontal component. Similarly, E_x is due to the charge on the gate and is the only component of the field due to the charge on the gate. Here, E_y varies with y but not with x; E_x assumes its maximum value at the source end of the channel and then $$\frac{\partial E_x}{\partial x} \approx \frac{E_x(0,y) - E_x(W,y)}{W} = \frac{E_x(0,y)}{W} \qquad (2.33)$$	CO1	K1
11a	Discuss in detail any four limits for low power design  Figure 2.19 Average power transfer during a switching transistor versus the transition interval.	CO1	K2
	OR		
11b	For CMOS inverter ,determine the expression for static power dissipation and dynamic power dissipation	CO1	K1

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

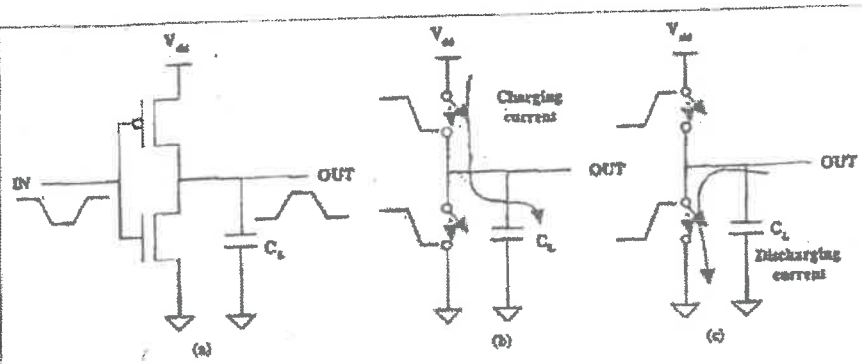


Figure 2.1. The operation of a CMOS inverter: (a) CMOS inverter, (b) Charging phase, and (c) Discharging phase.

PART C

(Answer all the Questions 1 x 10 = 10 Marks)

12a	Explain the optimization techniques for combinational circuits **Combinational Circuits Technology-Independent Optimization** **Two-Level Logic Circuits** Recently, some methods for optimizing two-level combinational circuits for low-power have been presented. In [19] employing the statistical characteristics of the input signals, a method that modifies the Expand routine of Espresso has been proposed. A new cost-function was introduced for guiding the cube expansion so that a cover with reduced switching activity will be derived. However, there are some drawbacks: i) the static probability assumed to be equal to 0.5 for every input signal, ii) all input signals are spatiotemporallyuncorrelated, and iii) the power dissipation of the input signals is not taken into account.	CO2	K2

OR

12b	With example explain the importance of transistor sizing in power dissipation Appropriate sizing of the transistors in CMOS circuits can be applied for minimizing the power consumption under a given delay constraint. Two kinds of algorithms have been proposed for transistor size optimization : i) Algorithms that start with a circuit that satisfies the timing constraint and reduce the size of the gates to reduce power dissipation. ii) Algorithms that start by performing an initial power-optimal sizing on each gate. If the power minimal layout satisfies the delay constraint, the process is terminated. Otherwise, the power delay optimal sizing is applied to transistor sizes on the critical paths until the timing target is met. An algorithm of this type is presented in [33]. This algorithm is more complex than previous ones because it takes into account not only the power dissipation which is due to the charging of the circuit capacitance but also the short circuit power dissipation. Another interesting conclusion of [33] is that the active area is not a reliable indicator of the power consuimption of a circuit. It is shown that the power consumption of a CMOS circuit is a convex function of the active area and the objective of minimizing the power dissipation for a transistor sizing algorithm is different than that of minimizing the active area.	CO2	K2

Course Faculty

(Name /Sign / Date)

P. SANTHOSH SELVI

HoD

(Name /Sign / Date)

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING
IG VALLEY, MANIDANDAM, TIRUCHIRAPPALLI – 620 012
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
ACADEMIC YEAR 2021 – 2022 (EVEN SEMESTER)
STUDENTS MARK STATEMENT- CO BASED

SUBJECT CODE &TITLE: VL4291 & LOW POWER VLSI DESIGN

YEAR/SEM: I/II **MONTH & YEAR: AUGUST & 2022**

S.NO	REG NO	STUDENT NAME	CO1	CO2	TOTAL (60)	TOTAL (100)
1.	811221419001	ABARNA T	26	12	38	63
2.	811221419003	PREETHA M	15	5	20	40

MARKS RANGE:

<20	20-30	31-40	41-50	51-60	61-70	71-80	81-90	91-100
0	0	1	0	0	1	0	0	0

Total No.of Candidates Present	2
Total No.of Candidates Absent	NIL
Total No.of Students Pass	1
Total No. of Students Fail	1
Percentage of Pass	50%

STAFF INCHARGE **HoD/ECE** **PRINCIPAL**

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 622 012, India
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Internal Assessment Test Answer Book

Name	Aparna-T			**Year/ Semester/Section**	I/II/A
Batch No.	2021-2023	**Date/Session**	05/08/22	**Department**	VLSI DESIGN
Course code	VL4291	**Course Title**	Low Power VLSI Design		
Internal Assessment Test	**IAT 1** ☑	**IAT 2** ☐	**IAT 3** ☐	**Model** ☐	
Name and Signature of the Invigilator with date	Invade 8/8/22 M.NANDHINI				

Instruction to the Student: Put tick mark to the question attended in the column against question.

Part A			Part B / Part C					Total Marks
Q. No.	✓	Marks	Q. NO.	✓	a Marks	✓	b Marks	
1	✓	2	11	✓	10			10
2	✓	2	12			✓	9	9
3	✓	1½	13	✓	8			8
4	✓	1½	14					
5			15					
6			16					
7	✓	2					Total	27
8								
9	✓	2						
10								
Total		11						

38/60
Grand Total

10/8/22
(P. Santhana Selvi)
Name and Signature of the Examiner with date

To be filled by the examiner

Course Outcomes	1	2	3	4	5	6	Total
Marks allotted	38	22					60
Marks Obtained	26	12					38

IQAC Audit - Remarks

—

Name and Signature of the IQAC member

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India

(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ROOT CAUSE ANALYSIS

Name of the Faculty : Ms. P. Santhana Selvi
Degree & Program : M.E & VLSI DESIGN
IA Test : I/II/III/Model
Target : 100 %

Course Code & Name : VL4291 & Low Power VLSI Design
Semester & Section : II & A
University Exam/Month & Year: OCT/NOV 2022
Achieved : 50 %

S.NO	BATCH NO./ REG NO.	NAME OF THE STUDENT	CAUSES FOR FAILURE	SIGNATURE OF THE STUDENT WITH DATE	CORRECTIVE ACTION TAKEN	PREVENTIVE ACTION TAKEN	FOLLOWUP STATUS	REMARKS OF THE HOD
1.	811221419003	Preetha M	Health issue.	Preetha	Assignment given	Advised to take care	Progress monitored	Try to get avg marks.

Signature of the Faculty Member

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

M. Bhuvaneswari
Signature of the HoD/ECE

INDRA GANESAN COLLEGE OF ENGINEERING

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IQAC Academic Audit Form

ACADEMIC YEAR: 2021 – 2022 EVEN SEMESTER

Name of Department : ME VLSI DESIGN | Year / Sem / Sec : I / II / A | No. of Students Registered : 02

Details of Examination : ✓IA Test -1 / IA Test -2 / IA Test -3 / Model Test

S.No.	Course Code	List of Reg.No Verified	Course Log Book Verified (Y / N)	Course File Verified (Y / N)	No of students Attended	No of Absentees	No of Failures	Pass %	Remarks
1.	VL4251	811221419001, &	Y	Y	2	1	–	100%	–
2	VL4292	811221419001	Y	Y	2	–	1	50%	–
3	VL4291	811221419001	Y	Y	1	1	–	50%	Retest
4	VL4252	811221419001	Y	Y	2	–	–	100%	–
5	EL407	811221419001	Y	Y	2	–	–	100%	–
6	AX4092	811221419001	Y	Y	1	1	–	50%	Retest

Verified by

External Member Name and Signature:	K. Seetharaman & K. Suthakar
Internal Member Name and Signature:	V. Srinath &

Overall Remarks:

Instructed to conduct Retest for failure students

M. Bhuvaneswari
HoD/ ECE

IQAC Coordinator

Principal

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.