Indra Ganesan
COLLEGE OF ENGINEERING

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai
Accredited by NAAC with 'B+' Grade, 2(f) & 12B Status Institution by UGC
IG Valley, Madurai Main Road, Manikandam, Tiruchirappalli - 620012

NAAC DOCUMENTS

QUALITY INDICATOR FRAME WORK

CRITERION – 1

CURRICULAR ASPECTS

SUBMITTED BY

IQAC

INTERNAL QUALITY ASSURANCE CELL

INDRA GANESAN COLLEGE OF ENGINEERING

Criteria 1	Curricular Aspects	100

1.1 Curricular Planning and Implementation (20)

1.1.1 The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment

Table of Content

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PREFACE OF THE COURSE FILE

Batch	: **2018-2020**
Academic Year	: **2019-2020 / ODD**
Program	: **M.E(VLSI)**
Year & Semester	: **2nd Year / 3rd Semester**
Course Code	: **VL5301**
Name of the Course	: **Analog to digital interfaces**
Faculty in-charge	: **Mrs.P.Santhanaselvi , AP/ECE**

Signature of the Faculty in-charge

HoD / ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

VL5301 ANALOG TO DIGITAL INTERFACES

L T P C

3 0 0 3

OBJECTIVES

- To understand the importance of sampling the input analog signal for digitization and enabling circuit architectures
- To understand the principles of Analog to Digital and Digital to Analog conversion of signals.
- To understand the importance of calibration techniques for achieving precision during data conversion

UNIT I SAMPLE AND HOLD CIRCUITS 9

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.

UNIT II SWITCHED CAPACITOR CIRCUITS AND COMPARATORS 9

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

UNIT III DIGITAL TO ANALOG CONVERSION 9

Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.

UNIT IV ANALOG TO DIGITAL CONVERSION 9

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V PRECISION TECHNIQUES 9

Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.

TOTAL: 45 PERIODS

OUTCOMES:

- To be able to design Analog to Digital and Digital to Analog data converters based on data precision requirements

REFERENCE:

1. Behzad Razavi, "Principles of data conversion system design", S. Chand and company Ltd, 2000.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Faculty Time Table

Mrs.P.SANTHANASELVI, AP / ECE								
Day Order	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
I				VL5301				
II								
III					VL5301			
IV		VL5301						
V				VL5301				

S.Code	Title	Year / Branch	Hours
VL5301	ANALOG AND DIGITAL INTERFACES	II / M.E(VLSI)	4
TOTAL - 4 hours			

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Lecture Schedule

Degree/Program: **M.E / VLSI**
Duration: **Aug 2019 - Dec 2019**

Course code &Name: **VL5301 – Analog to Digital Interfaces**
Semester: **III** Section: **A** Faculty:**Mrs.P.Santhanaselvi**

AIM:

To teach the students about the analysis of various types of Analog to digital interfaces

OBJECTIVES:

To impart knowledge on

(i) To analyse the importance of sampling the input analog signal for digitization and enabling circuit architectures.
(ii) To analyse the principles of Analog to Digital and Digital to Analog conversion of signals.
(iii) To analyse the importance of calibration techniques for achieving precision during data conversion

PREREQUISITES:

COURSE OUTCOMES:

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C201.1	Describe about Sample and hold circuits	1,3,5,6,12	3
C201.2	Explain about the Switched capacitor circuits and comparators	1,3,6,12	2
C201.3	To be able to design Digital to Analog data converters based on data precision requirements	1,2,5,6,12	1
C201.4	To be able to design Analog to Digital data converters based on data precision requirements	1,2,5,6,12	2,3
C201.5	To know about the Precision Techniques	1,2,4,5,6,12	2,3
C201.6	To know about the sigma-delta analog-to-digital and digital-to-analog converters	1,3,5,6	1,2

S.No	Date	Period	Topics to be Covered	Book & Page. No.
UNIT -I - SAMPLE AND HOLD CIRCUITS				**Target periods :9**
1	22/08/19	4	Sampling switches	T1
2	22/08/19	7	Conventional open loop and closed loop sample and hold architecture	T1
3	25/08/19	4	Open loop architecture with miller compensation	T1
4	26/08/19	1	multiplexed input architectures	T1
5	26/08/19	7	recycling architecture	T1
6	29/08/19	4	recycling architecture	T1
7	29/08/19	7	switched capacitor architecture	R1
8	01/09/19	4	switched capacitor architecture	R1
9	02/09/19	1	QUIZ-1	Material
UNIT II - SWITCHED CAPACITOR CIRCUITS AND COMPARATORS				**Target periods :9**
10	08/09/19	4	Switched-capacitor amplifiers	T1

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11	09/09/19	1	switched capacitor integrator	T1
12	09/09/19	7	switched capacitor common mode feedback	T1
13	12/09/19	4	switched capacitor common mode feedback	T1
14	12/09/19	7	Single stage amplifier as comparator	R1
15	15/09/19	4	cascaded amplifier stages as comparator	R1
16	16/09/19	1	latched comparators	R1
17	16/09/19	7	latched comparators	T1
18	19/09/19	4	QUIZ-II	Material
UNIT III - DIGITAL TO ANALOG CONVERSION				**Target Periods :9**
19	23/09/19	7	Performance metrics	T1
20	26/09/19	4	reference multiplication and division	T1
21	26/09/19	7	reference multiplication and division	T1
22	29/09/19	4	switching and logic functions in DAC	T1
23	30/09/19	1	switching and logic functions in DAC	T1
24	30/09/19	7	Resistor ladder DAC architecture	T1
25	03/10/19	4	Resistor ladder DAC architecture	R1
26	03/10/19	7	current steering DAC architecture	R1
27	06/10/19	4	QUIZ-III	Material
UNIT IV - ANALOG TO DIGITAL CONVERSION				**Target Periods :9**
28	10/10/19	7	Performance metrics	T1
29	13/10/19	4	Flash architecture	T1
30	14/10/19	1	Flash architecture	T1
31	14/10/19	7	Pipelined Architecture	T1
32	17/10/19	4	Pipelined Architecture	T1
33	17/10/19	7	Successive approximation architecture	R1
34	20/10/19	4	Successive approximation architecture	R1
35	21/10/19	1	Time interleaved architecture.	R1
36	21/10/19	7	Time interleaved architecture.	R1
UNIT V - PRECISION TECHNIQUES				**Target Periods:9**
37	31/10/19	4	Comparator offset cancellation	T1
38	31/10/19	7	Comparator offset cancellation	T1
39	03/11/19	4	Op Amp offset cancellation	T1
40	04/11/19	1	Op Amp offset cancellation	T1
41	04/11/19	7	Calibration techniques	T1
42	07/11/19	4	Calibration techniques	T1
43	07/11/19	7	range overlap	T1
44	10/11/19	4	range overlap	R1
45	11/11/19	1	digital correction	R1
Content Beyond the Syllabus				
46	17/11/19	4	Oversampling sigma-delta analog-to-digital and digital-to-analog converters	Material

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Book Reference- References

Sl	Title of the Book	Author	Publisher	Year
1.	Principles of data conversion system design	Behzad Razavi	S. Chand and company Ltd	2000

Website Reference:

http://nptel.iitm.ac.in/courses.php?branch=Electronics

www.freebookspot.com

Signature of the Faculty in-charge

HoD / ECE

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Identification of Curricular Gap & Content Beyond Syllabus(CBS)

Name of the Faculty :Mrs.P.Santhanaselvi **Course Code & Name:VL5301-Analog to digital interfaces**

Degree & Program:M.E. /VLSI **Semester & Section: III / A** **Academic Year: 2019 -2020 /ODD**

I.Mapping of Course Outcomes with POs & PSOs.(before CBS)

Table.1 Mapping of COs, C, PSOs with POs - before CBS.

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C201.1	3	-	3	-	3	2	-	-	-	-	-	3	-	-	1
C201.2	3	-	3	-	-	2	-	-	-	-	-	3	-	3	-
C201.3	3	3	-	-	3	2	-	-	-	-	-	3	2	-	-
C201.4	3	3	-	-	3	2	-	-	-	-	-	3	-	3	1
C201.5	3	3	-	3	3	2	-	-	-	-	-	3	-	3	1
C201.6	3	-	3	-	3	2	-	-	-	-	-	-	2	3	-
C201	3	3	3	3	3	2	-	-	-	-	-	3	2	3	1

II. Identification of content beyond syllabus.

Table.2 Identification of content beyond syllabus

Details of Content Beyond Syllabus(CBS) added	POs strengthened/ vacant filled	CO/Unit
Oversampling sigma-delta analog-to-digital and digital-to-analog converters	PO2,PO12 vacant filled	C201.6/ III & IV

III. Mapping of Course Outcomes with POs & PSOs. (After CBS)

Table.3 Mapping of COs, C, PSOs with POs- after CBS.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C203.1	3	-	3	-	3	2	-	-	-	-	-	3	-	-	1
C203.2	3	-	3	-	-	2	-	-	-	-	-	3	-	3	-
C203.3	3	3	-	-	3	2	-	-	-	-	-	3	2	-	-
C203.4	3	3	-	-	3	2	-	-	-	-	-	3	-	3	1
C203.5	3	3	-	3	3	2	-	-	-	-	-	3	-	3	1
C203.6	3	*3	-	-	-	-	-	-	-	-	-	*3	-	-	-
C203	3	3	3	3	3	2	-	-	-	-	-	3	2	3	1

Signature of the Faculty

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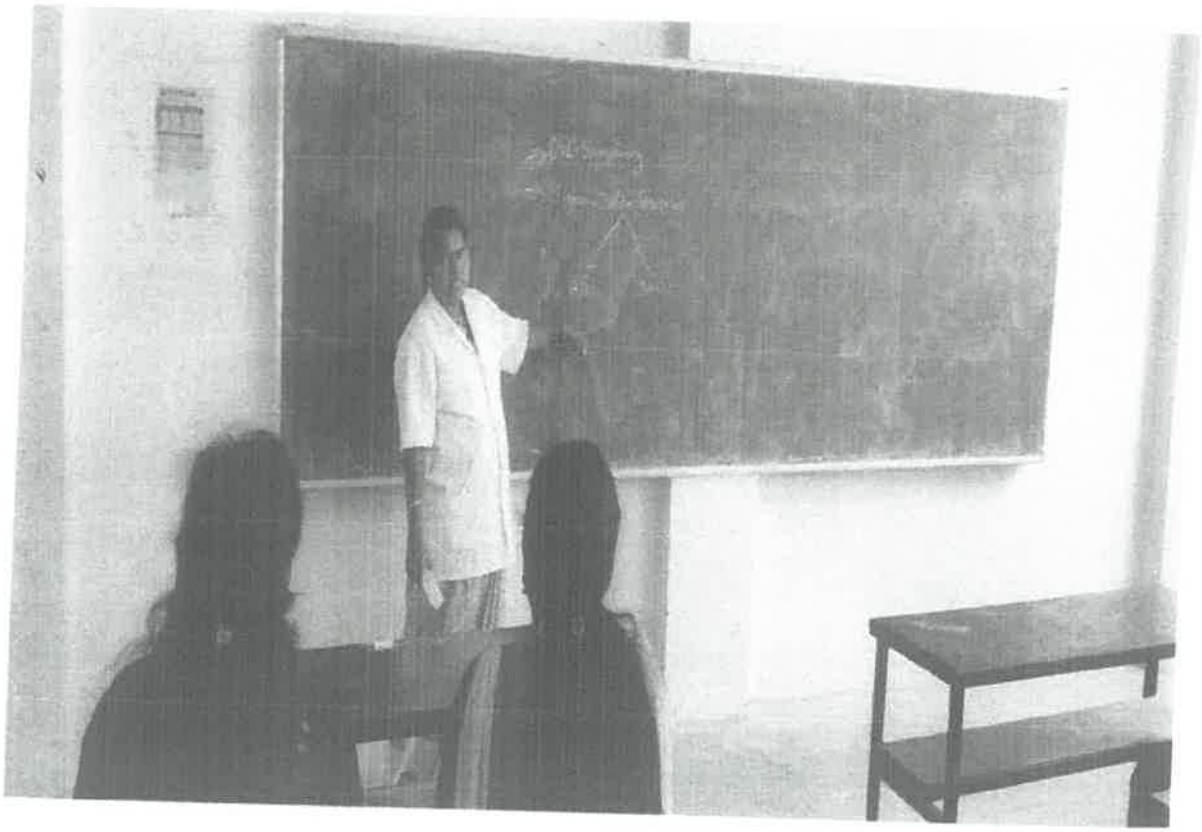
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Proof of Curricular Gap & Content Beyond Syllabus(CBS)

Name of the Faculty : Mrs.P.Santhanaselvi **Course Code&Name:VL5301-Analog to digital interfaces**

Degree & Program:M.E. /VLSI **Semester & Section: III/A** **Academic Year: 2019 -2020 /ODD**



Signature of the Faculty

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Proof of Curricular Gap & Content Beyond Syllabus(CBS)

Name of the Faculty : Mrs.P.Santhanaselvi *Course Code&Name:VL5301-Analog to digital interfaces*

Degree & Program:M.E. /VLSI *Semester & Section: III/A* *Academic Year: 2019 -2020 /ODD*

Over Sampling Sigma Delta analog to digital and digital to analog converters

- Delta-sigma modulation is used in analog-to-digital converters and digital-to-analog converters.
- The advantage of oversampling in delta-sigma modulation is that the quantization noises are spread over a larger frequency range, reducing the quantization noise spectral density.
- In delta-sigma analog-to-digital converters, the digital decimation filter increases data resolution and removes the quantization noise that is outside the frequency band of interest. It also determines the signal bandwidth, settling time, and stop band rejection.

Sigma-Delta Conversion:

- Oversampling and noise shaping focuses on achieving high signal-to-noise-ratio (SNR) in a limited frequency band without reducing the data rate of the signal. This technique results in the efficient digital transmission of signals. The combination of oversampling and noise shaping is the basic underlying principle of delta-sigma modulation.
- Delta-sigma modulation is used in analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). In ADCs, the delta-sigma modulator features all the merits of oversampling and noise shaping along with a digital decimation filter.
- Let's take a closer look at the concept of delta-sigma modulation.

- The Basic Principles of Delta-Sigma Modulation
- Delta-sigma modulation, otherwise called sigma-delta modulation, is used in digital signal processing and signal conversion to improve the resolution and SNR of signals. These techniques are extensively used in portable audio playback devices, mobile phones, analog-to-digital converters, and digital-to-digital converters. The basic principles of delta-sigma modulation are oversampling and noise shaping.

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Over Sampling:

- The sampling process follows the Nyquist-Shannon criteria, where the sampling frequency should be at least twice the maximum analog signal frequency. In the oversampling process, samples per second are more than what is required, according to Nyquist-Shannon criteria. Allowing more sample rates does not influence the signal power and total quantization noise power. Therefore, the SNR remains unchanged.
- The advantage of oversampling is that the quantization noises are spread over a larger frequency range. This reduces the quantization noise spectral density (the SNR over the frequency of interest is increased). Comparing normal sampling and oversampling, the quantization noise power is reduced by 3 dB for every doubling of oversampling ratio (OSR), where OSR is the ratio of sampling frequency to twice the frequency of the signal.

Noise Shaping:

- Noise shaping is the second step of delta-sigma modulation. This is where the signal to quantization noise ratio is increased by altering the frequency distribution. The frequency band is reduced to the signal band so that the quantization noise density is reduced and the SNR is increased in the low-frequency area of the spectrum. Noise shaping increases the noise density at frequencies outside the signal band.
- In delta-sigma modulators, noise shaping is realized with an error minimizing the feedback loop. It minimizes the error between the input signal (x) and the quantized output signal (y). The feedback loop compares the input signal and the quantized output signal, and the difference between them that lies within the signal band is passed to the output side without attenuation. The out-of-the-band differences are suppressed using a filter. The result of the weighing is passed to the quantizer, which generates the next output value. The output signal generated is again fed back to the loop for the next comparison, and this continues until a close match between the input signal and the output signal is obtained in the signal passband.

Digital and Decimation Filters in Delta-Sigma ADCs:

- In delta-sigma modulators used for analog-to-digital conversion, the digital and decimation filter extracts information from the sampled data and reduces the data rate to a more useful range. It increases the data resolution and removes the quantization noise that is outside the frequency band of interest. It is the decimation filter block that determines the signal bandwidth, settling time, and stopband rejection in delta-sigma ADCs.
- Oversampling and noise shaping in any delta-sigma modulation increases its efficiency, as the quantization noise is outside the scope of the signal band of interest. Delta-sigma modulation offers high resolution, high SNR, low power consumption, and low-cost ADCs and DACs for applications like process control and physical quantity measurements such as temperature and pressure.

Sigma-delta ADCs/ Over sampling Converters:

- It consists of 2 main parts - modulator and digital filter. The modulator includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The modulator oversamples the input signal, converting it to a serial bit stream with a frequency much higher than the required sampling rate. This is then transformed by the output filter to a sequence of parallel digital words at the sampling rate. The characteristics of sigma-delta converters are high resolution, high accuracy,

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- Low noise and low cost.
- Typical applications are for speech and audio.
- A **Sigma-Delta ADC** (also known as a Delta-Sigma ADC) oversamples the desired signal by a large factor and filters the desired signal band. Generally a smaller number of bits than required are converted using a Flash ADC after the Filter. The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies.
- A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output. (sigma-delta modulation, also called delta-sigma modulation)

Signature of the faculty

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Assignment Answer Sheet

Name of the Student : M.Vel Rajeswari

AU Register Number: 811218419003

Assignment – 01			Date of Issue:	04.09.2022	Marks	10
Course code	VL5301	Course Title	Analog to digital interfaes			
Year	II	Semester/Section	III / A	Date of Submission:	08.09.2022	

Q.No	Questions	CO
1.	Conventional open loop and closed loop sample and hold architecture	C201.1
2.	switched capacitor architecture	C201.1

Mark Allocation

Rubrics	Marks Allocated	Marks obtained
Content Quality	6	4
Presentation Quality	2	2
Timely submission	2	2
Total marks	10	8

Name and Signature of the Faculty Incharge

P. SANTHANA SELVI

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Register Number:

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Internal Assessment Exam - I						
Course code	VL5301	Course Title	Analog to digital interfaces	Date/Session	14.10.19/FN	Marks 60
Regulation	2017	Duration	90 minutes	Academic Year	2019-2020	
Year	II	Semester	III	Department	M.E(VLSI)	

COURSE OUTCOMES

CO1:	Describe about Sample and hold circuits
CO2:	Explain about the Switched capacitor circuits and comparators
CO3:	To be able to design Digital to Analog data converters based on data precision requirements
CO4:	To be able to design Analog to Digital data converters based on data precision requirements
CO5:	To know about the Precision Techniques
CO6:	To know about the sigma-delta analog-to-digital and digital-to-analog converters

Q.No.	Question	CO	BTS
	PART A (Answer all the Questions 9 x 2 = 18 Marks)		
1	Define Sampling switch	CO1	K1
2	Differentiate Open loop & closed loop sample and hold architecture	CO1	K4
3	What is Miller compensation?	CO1	K2
4	Define multiplexed input architecture.	CO1	K1
5	What is recycling architecture?	CO1	K2
6	Define switched capacitor architecture	CO1	K2
7	Define switched capacitor amplifiers	CO2	K2
8	What is switched capacitor integrator?	CO2	K1
9	What is latched comparators?	CO2	K2
	PART B (Answer all the Questions 2 x 14 = 28 Marks)		
11a	Explain about the Conventional open loop and closed loop sample and hold architecture	CO1	K3
	OR		
11b	Explain about the Open loop architecture with miller compensation	CO1	K3
12a	Explain about the switched capacitor architecture.	CO1	K3
	OR		
12b	Explain in detail about the Sampling switches	CO1	K3
	PART C (Answer all the Questions 1 x 14 = 14 Marks)		
13a	Explain in detail about the switched capacitor common mode feedback	CO2	K3
	OR		
13b	Explain in detail about the switched capacitor integrator	CO2	K3

Course Faculty 11/10/19

(Name /Sign / Date)

P SANTHANA LAKSHMI

HoD

(Name /Sign / Date)

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RTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2019 – 2020 (ODD SEMESTER)

STUDENTS MARK STATEMENT- CO BASED

INTERNAL ASSESSMENT-I

SUBJECT CODE &TITLE: VL5301 – Analog to digital interfaces

YEAR/SEM: II/III **MONTH & YEAR: OCT 2019**

S.NO	REG NO	STUDENT NAME	CO1	CO2	TOTAL (60)	TOTAL (100)
1.	811218419002	Shalini K	35	10	45	77
2.	811218419003	Vel Rajeswari M	30	8	38	71

MARKS RANGE:

<20	20-30	31-40	41-50	51-60	61-70	71-80	81-90	91-100
0	0	0	0	0	0	2	0	0

Total No.of Candidates Present	2
Total No.of Candidates Absent	0
Total No.of Students Pass	2
Total No. of Students Fail	0
Percentage of Pass	100

STAFF INCHARGE

HoD/ECE

PRINCIPAL

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IQAC Academic Audit Form

ACADEMIC YEAR: 2019-2020 ODD SEMESTER

Name of Department :	M.E (VLSI)	Year / Sem / Sec :	/ /A	No. of Students Registered :	2

Details of Examination : IA Test -1 / IA Test -2 / IA Test -3 / Model Test

S.No.	Course Code	List of Reg.No Verified	Course Log Book Verified (Y / N)	Course File Verified (Y / N)	No of students Attended	No of Absentees	No of Failures	Pass %	Remarks
1.	VL5301	811218419003	Y	Y	2	–	–	100%	–
2.	AP5292	811218419002	Y	Y	2	–	–	100%	–
3.	VL5012	811218419003	Y	Y	2	–	–	100%	–

Verified by

External Member Name and Signature:	D. Praveen Sangeeth kumar &
Internal Member Name and Signature:	J. Manokaran &

Overall Remarks:

–

HoD / ECE

IQAC Co-ordinator

Principal

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Internal Assessment Test Answer Book

Name	K. Shalini			Year/ Semester/Section	II/III
Batch No.	8112184190002	Date/Session	14/10/19-FN	Department	M.E.(VLSI)
Course code	VL 5301	Course Title	Analog to Digital interfaces.		
Internal Assessment Test		IAT 1 ☑	IAT 2 ☐	IAT 3 ☐	Model ☐
Name and Signature of the Invigilator with date					

Instruction to the Student: Put tick mark to the question attended in the column against question.

Part A			Part B / Part C						Total Marks
Q. No.	✓	Marks	Q. NO.	✓	a Marks	✓	b Marks		
1		2	11		12				12
2		2	12		10				10
3		1	13		10				10
4		1	14						
5		2	15						
6		1	16						
7		1						Total	32
8		2	FOUR FIVE						
9		1	45/60						
10		—							
Total		13	Grand Total						

D. SANTHANASELVI.

15/10/19
Name and Signature of the Examiner with date

To be filled by the examiner							
Course Outcomes	1	2	3	4	5	6	Total
Marks allotted	40	20					60
Marks Obtained	35	10					45
IQAC Audit - Remarks							

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Name and Signature of the IQAC member

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
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