INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PREFACE OF THE COURSE FILE

Batch : **2018-2020**

Academic Year : **2018-2019 / EVEN**

Program : **PG- M.E –VLSI Design**

Year & Semester : **IYear / II Semester**

Course Code : **AP5191**

Name of the Course : **Embedded System Design**

Faculty in-charge : **Mr.K.Kumar AP/ECE**

Signature of the Faculty in-charge

HoD / ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
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Manikandam, Trichy-620 012.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Faculty Time Table

Mr.K.Kumar								
Day Order	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
I		**AP5191**						**AP5191**
II			**AP5191**					
III								
IV					**AP5191**			
V								

S.Code	Title	Year / Branch	Hours
AP5191	Embedded System Design	I/M.E VLSI DESIGN	4
TOTAL - 4 hours			

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AP5191 EMBEDDED SYSTEM DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES :

The students should be made to:

Learn design challenges and design methodologies

- Study general and single purpose processor
- Understand bus structures

UNIT I EMBEDDED SYSTEM OVERVIEW 9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors. 33

UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR 9

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer"s view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III BUS STRUCTURES 9

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11.

UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS 9

Basic State Machine Model, Finite-State Machine with Datapath Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification : Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models.

UNIT V EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS 9

Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS – System design using RTOS.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

C113.1 : Explain different protocols.

C113.2 : Discuss state machine and design process models.

C113.3 : Explain the functions of Microcontroller .

C113.4 : Learn the functions of Different Bus interface.

C113.5 : Discuss the State machine models.

C113.6 : Outline embedded software development tools and RTOS.

REFERENCES:

1. Bruce Powel Douglas, "Real time UML, second edition: Developing efficient objects for embedded systems", 3rd Edition 1999, Pearson Education.

2. Daniel W. Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education, 2002.

3. Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & sons, 2002.

4. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004

CO's-PO's & PSO's MAPPING

CO	PO 1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO 2	PSO 3
C113.1	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3
C113.2	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3
C113.3	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3
C113.4	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3
C113.5	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3
C113.6	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3

1- Low, 2- Medium, 3- high, - no correlation

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Lecture Schedule

Degree/Program: **M.E / VLSI Design** Course code &Name: **AP5191– Embedded System Design**

Duration: **Jan 2019 - April 2019** Semester: **II** Section: **A** Faculty: **Mr.K.Kumar**

AIM:

To teach the students about the various types of Microprocessor Architecture and Interfacing Ics.

OBJECTIVES:

To impart knowledge on

C113.1 : Explain different protocols.

C113.2 : Discuss state machine and design process models.

C113.3 : Explain the functions of Microcontroller .

C113.4 : Learn the functions of Different Bus interface.

C113.5 : Discuss the State machine models.

C113.6 : Outline embedded software development tools and RTOS.

PREREQUISITES:

COURSE OUTCOMES:

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C113.1	Explain different protocols.	1,2,3,4,5,6,11,12	1,2,3
C113.2	Discuss state machine and design process models.	1,2,3,4,5,6,11,12	1,2,3
C113.3	Explain the functions of Microcontroller .	1,2,3,4,5,6,11,12	1,2,3
C113.4	Learn the functions of Different Bus interface.	1,2,3,4,5,6,11,12	1,2,3
C113.5	Discuss the State machine models.	1,2,3,4,5,6,11,12	1,2,3
C113.6	Outline embedded software development tools and RTOS.	1,2,3,4,5,6,11,12	1,2,3

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S.No	Date	Period	Topics to be Covered	Book & Page. No.
			UNIT I EMBEDDED SYSTEM OVERVIEW	**Target periods :0**
1	19.01.2019	5	Embedded System Overview	T1
2	20.01.2019	2	Design Challenges	T1
3	20.01.2019	7	Optimizing Design Metrics	T1
4	21.01.2019	3	Design Methodology	T1
5	24.01.2019	5	RT-Level Combinational Components	T1
6	28.01.2019	2	RT-Level Combinational Components	T1
7	28.01.2019	7	RT-Level Sequential Components	T1
8	29.01.2019	3	RT-Level Sequential Components	T1
9	31.01.2019	5	Optimizing Custom Single-Purpose Processors	T1
10	01.02.2019	5	Optimizing Custom Single-Purpose Processors	T1
			UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR	**Target Periods :0**
11	02.02.2019	2	Basic Architecture of processor	T1
12	02.02.2019	7	Pipelining, Superscalar and VLIW architectures	T1
13	04.02.2019	2	Programmer"s view, Development Environment	T1
14	04.02.2019	7	Application-Specific Instruction-Set Processors (ASIPs)	T1
15	05.02.2019	3	Microcontrollers	T1
16	07.02.2019	5	Timers, Counters and watchdog Timer	T1
17	09.02.2019	3	UART	T1
18	11.02.2019	2	LCD Controllers	T1
19	11.02.2019	7	Analog-to-Digital Converters	T1
20	12.02.2019	3	Memory Concepts	NPTEL
			UNIT III BUS STRUCTURES	
23	14.02.2019	5	Basic Protocol Concepts	T1
24	18.02.2019	2	Microprocessor Interfacing	T1
25	18.02.2019	7	I/O Addressing	T1
26	19.02.2019	3	Port and Bus-Based I/O	T1
27	21.02.2019	5	Bus Arbitration	T1
28	25.02.2019	2	Serial Protocols	T1
29	25.02.2019	7	I2C, CAN and USB	T1
30	26.02.2019	3	Parallel Protocols – PCI and ARM Bus	T1
31	28.02.2019	5	Wireless Protocols – IrDA, Bluetooth, IEEE 802.11	T1
			UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS	**Target Periods:0**
33	07.03.2019	5	Basic State Machine Model	T2
34	09.032019	2	Finite-State Machine with Datapath Model	T2
35	09.03.2019	7	Capturing State Machine in Sequential Programming Language	T2
36	11.03.2019	2	Program-State Machine Model	T2
37	11.03.2019	7	Concurrent Process Model	T2
38	12.03.2019	3	Communication among Processes	T2
39	14.03.2019	5	Synchronization among processes	T2
40	18.03.2019	2	Real-time Systems	T2
41	18.03.2019	7	Automation: Synthesis, Verification : Hardware/Software Co-Simulation	T2
42	19.03.2019	3	Reuse: Intellectual Property Cores, Design Process Models.	T2
			UNIT V EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS	**Target Periods:0**

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43	21.03.2019	5	Compilation Process	T2
44	23.03.2019	5	Libraries	T2
45	25.03.2019	2	Porting kernels	T2
46	25.03.2019	7	C extensions for embedded systems	T2
45	26.03.2019	3	emulation	T2
46	28.03.2019	5	debugging techniques	T2
47	01.04.2019	2	debugging techniques	T2
48	01.04.2019	7	RTOS	T2
49	02.04.2019	3	System design using RTOS	T2
50	04.04.2019	5	System design using RTOS	T2
Content Beyond the Syllabus				
67	04/06/22		Washing Machine	Material

Book Reference - Text Books

Sl.	Title of the Book	Author	Publisher	Year
1.	"Real time UML, second edition: Developing efficient objects for embedded systems" .	Bruce Powel Douglas	Second 3rd Edition Pearson Education.	1999
2	"Fundamentals of embedded software where C and assembly meet" ||	Daniel W. Lewis	Pearson Education	2002

Book Reference- References

Sl	Title of the Book	Author	Publisher	Year
1.	"Embedded System Design"	Frank Vahid and Tony Gwargie	John Wiley & sons	2002
2.	"Embedded System Design"	Steve Heath	Elsevier, Second Edition	2004

Signature of the Faculty in-charge

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Identification of Curricular Gap & Content Beyond Syllabus(CBS)

Name of the Faculty :Mr.K.Kumar **Course Code & Name: AP5191– Embedded System Design**
Degree & Program:M.E. / VLSI Design **Semester & Section: II / A** **Academic Year: 2018 -2019 /EVEN**

I.Mapping of Course Outcomes with POs & PSOs.(before CBS)

Table.1 Mapping of COs, C, PSOs with POs - before CBS.

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C113.1	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3
C113.2	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3
C113.3	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3
C113.4	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3
C113.5	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3
C113.6	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3
C113	3	3	3	2	2	3	-	-	-	-	2	1	1	2	3

II. Identification of content beyond syllabus.

Table.2 Identification of content beyond syllabus

Details of Content Beyond Syllabus(CBS) added	POs strengthened/ vacant filled	CO/Unit
Washing Machine	PO4,PO12 Strengthened	C113.6/ IV & V

III. Mapping of Course Outcomes with POs & PSOs. (After CBS)

Table.3 Mapping of COs, C, PSOs with POs- after CBS.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C113.1	3	3	3	3	2	3	-	-	-	-	2	3	1	2	3
C113.2	3	3	3	3	2	3	-	-	-	-	2	3	1	2	3
C113.3	3	3	3	3	2	3	-	-	-	-	2	3	1	2	3
C113.4	3	3	3	3	2	3	-	-	-	-	2	3	1	2	3

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C113.5	3	3	3	3	2	3	-	-	-	-	2	3	1	2	3
C113.6	3	3	3	3	2	3	-	-	-	-	2	3	1	2	3
C113	3	3	3	3	2	3	-	-	-	-	2	3	1	2	3

Signature of the Faculty

HoD/ECE

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Washing machine Controller

The quality and quantity of clothes to be washed are measured with a detecting unit, the measured values are referenced to cloth quantity and quality Fuzzy functions to control the strength of wash current, wash time, and rinse time so as to be suitable for the quantity and type of clothes to be washed.

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a controller for controlling the operation of a washing machine so as to achieve an optimum washing operation by detecting the quantity and type of clothes.

2. Description of the Prior Art

A conventional washing machine determines the water current and wash time in accordance with the quantity of clothes to be washed. For example, if the quantity of clothes is small, they are washed with a soft water current for less time. On the contrary, if the quantity of clothes is large, they are washed with a strong water current for a long time.

Therefore, if a small quantity of large-sized clothes such as sheets and bath towels is washed, the cleaning power of the washing machine is weak. On the other hand, if a lot of thin clothes such as lingerie is washed, there is a fear of spoiling them in the washing.

SUMMARY OF THE INVENTION

It is an object of the present invention to eliminate the above disadvantage and provide a controller for controlling the operation of a washing machine so as to achieve a water current strength and wash time suitable for the quantity and quality of clothes to be washed.

It is another object of the present invention to provide a controller for controlling the operation of a washing machine so as to achieve a water current strength, wash time, and rinse time, suitable for the quantity and quality of clothes to be washed.

It is another object of the present invention to provide a controller for controlling the operation of a washing machine so as to achieve a water current strength, wash time, rinse time, and water extract time, suitable for the quantity and quality of clothes to be washed.

In order to achieve the above object of this invention, the quality and quantity of clothes to be washed are measured with a detecting means, the measured values are referenced to cloth stored quantity and quality Fuzzy functions to calculate the strength of wash current, and wash time, to thereby achieve an optimum operation of the washing machine.

More in particular, membership functions according to the Fuzzy theory are defined for the cloth quantity and type, the strength of water current, for example. Rules are defined for the washing conditions such as large or small cloth quantity, large-sized or thin cloth type, strong or weak water current, and so on. Each rule is executed using the Fuzzy theory to thereby achieve an optimum operation of the washing machine.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings illustrate a particular structure of an embodiment of the controller according to the present invention.

FIG. 1 is a cross sectional view showing a completely automatic washing machine;

FIG. 3 is a circuit diagram of detecting means for detecting the quantity and quality of clothes;

FIG. 4 shows pulses detected by the detecting means shown in FIG. 3;

FIG. 5 is a graph showing the interval between pulses detected by the detecting means;

FIG. 6 is a diagram conceptually illustrating the cloth quantity Fuzzy function;

FIG. 7 is a diagram conceptually illustrating the cloth quality Fuzzy function;

FIG. 8 is a diagram conceptually illustrating the water current Fuzzy function; and

FIG. 9 are diagrams illustrating Fuzzy inference rules.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A particular structure of an embodiment of the controller according to the present invention will be described.

Referring to FIG. 1 within an outer frame 1 made of steel plate, an outer tub 4 made of synthetic resin is suspended by means of vibration proofing units 3 each being constructed of a suspending rod 2, coil spring, elastic rubber, for example. There are provided four vibration proofing units 3.

A washing/water-extract tub 5 made of synthetic resin is rotatably mounted within the outer tub 4, water being supplied within the washing/water-extract tub 5 and outer tub 4. A number of water extract holes 5a are formed in the washing/water-extract tub 5. At the center of the bottom of the washing/water-extract tub 5, there is rotatably mounted a rotary member 6 like a pulsator or an agitator. During a washing process and rinsing process, the washing/water-extract tub 5 is stopped and the rotary member 6 is rotated in the clockwise and counter clockwise directions. During a water extract process, the washing/water-extract tub 5 is rotated in one direction. The rotary member 6 and washing/water-extract tub 5 are rotated by means of a driver unit 7.

The driver unit 7 is constructed of a motor 8, a transmission means 9, a clutch unit 10, a solenoid 7a, and a water drainage unit 12. The transmission means 9 is constructed of a pulley 9a and a belt 9b, and transmits the rotation of the motor 8 to the rotary member 6 or washing/water-extract tub 5. The clutch unit 10 is switched by the solenoid 7a in order that only the rotary member 6 is rotated during the washing and rinsing processes or the washing/water-extract tub 5 is rotated during the water extract process. The water drainage unit 12 operates to drain water.

The driver unit 7 is fixedly mounted on a support plate 14 of steel plate near at the bottom surface of the outer tub 4. The outer tub 4 is formed with a guide port 4c to which an air tube 4d is coupled to transmit the water pressure within the outer tub 4 to a water level sensor 26.

A top cover 19 made of synthetic resin is mounted at the top of the outer frame 1. The top cover 19 is formed with an opening 19a for entering washing clothes into the washing/water-extract tub 5, and an operation box 19b for housing therein electrical components such as a controller unit. There is provided a lid 20 made of synthetic resin for covering the opening 19a.

An operation panel 21 is mounted on the upper surface of the operation box 19b. A water supply electromagnetic valve 24 is mounted within the operation box 19b.

The water level sensor 26 disposed within the operation box 19b detects the water pressure within the outer tub 4 to thereby judge if water has been supplied to a predetermined water level. The water level sensor 26 is constructed of a core, a coil, a spring, for example.

Within a housing box 31, there is disposed the controller unit for controlling the washing, rinsing, water extracting, and other processes.

The operation panel 21 is equipped with a power switch button 29 and external operation switches 30.

FIG. 2 shows the operation panel 21.

With the washing machine constructed as above, when the power switch button 29 is depressed to turn on the power switch and a "sensor standard" button for one of the external operation switches is depressed, the water supply electromagnetic valve 24 is powered in response to a signal from the controller unit so that water is supplied to the washing/water-extract tub 5. The solenoid 7a is also powered at this time such that the motor is powered on for 0.5 second and off for 4 seconds. As a result, the washing/water-extract tub 5 rotates slowly in one direction to thereby allow water to be distributed uniformly over the washing clothes. In this case, the clutch unit is set similar to the case of the water extract process.

When the water level sensor 26 detects the lowest water level set for initial water supply, the water supply electromagnetic valve 24 and solenoid 7a are turned off and the motor 8 is powered to start agitating. In this case, the clutch unit 10 is correctly switched from the water extract process state to the washing process state. The motor 8 is driven for 8 seconds such that the rotary member 6 is reciprocally rotated to produce an alternate agitating water current while turning on for 0.5 second and off for 0.5 second, the strength of this alternating water current being stronger than that during the cloth quantity detection process and weaker than that during ordinary agitating so as not to spoil the washing clothes. This 8 second operation is a running-in operation before the cloth quantity detection process.

During the cloth quantity detection process, the rotary member 6 is reciprocally rotated for producing alternate agitating current while turning on for 0.4 second and off for 1 second. The counter electromotive force of the motor 8 rotating by its inertial force during the off-period is detected as a voltage across a driver capacitor 8a of the motor 8. This detected voltage is converted into d.c. rectangular pulses. A time duration tl between pulses is measured to determine the cloth quantity. If the quantity of clothes is large, a large resistance is applied to the rotary member 6 and the rotation of the motor by the inertial force is suppressed, thereby resulting in a longer time duration tl. On the other hand, if the quantity of clothes is small, the time duration tl between pulses becomes shorter. There is measured the time duration tl between the rise times of the first and third pulses (A) and (C) detected by the circuit shown in FIG. 3 (refer to FIG. 4). This measurement is repeated 20 times. The total time is used for determining the cloth quantity while referring to the relationship between cloth quantity and total time previously stored in a microcomputer within the control unit. The water level for the determined cloth quantity is automatically set to supply water to a rated water level.

The cloth quantity detection process is repeated to measure the pulse rise time intervals tl at various water levels until water is supplied to the rated water level. For example, the pulse rise time intervals tl at various water levels may be represented by curves shown in FIG. 5 for different washing clothes of 4.0 Kg (for large-size clothes such as sheets, bath towels, and for light-weighted clothes such as thin clothes made of chemical fibers). It is possible to discriminate between the types of clothes (cloth quality) by:

(1) calculating a difference ΔT between tl at the lowest and rated water levels (large-size clothes $\Delta T1$>thin clothes $\Delta T2$), and

(2) obtaining an approximate function of each curve of FIG. 5. It is therefore possible to wash clothes at an automatically set suitable water current, wash time, rinse time and the like (large-size clothes are washed at a strong water current for a long time, whereas thin clothes are washed at a weak water current for a short time).

Using the Fuzzy theory, it becomes possible to wash clothes in the manner as many housewives do, by incorporating the data regarding the cloth quantity (large, medium, small) and cloth type (large-size, standard, thin) into Fuzzy functions which are stored in the microcomputer of the controller and setting a water current (on/off time and speed of motor) and wash time.

For example, the membership function (hereinafter called a Fuzzy function) according to the Fuzzy theory for the cloth quantity can be described as shown in FIG. 6. The Fuzzy function for the cloth type or cloth quality can be described as shown in FIG. 7. The Fuzzy function used for controlling the strength of the water current in accordance with the cloth quantity and type or quality can be given as shown in FIG. 8. The following rules are defined for the Fuzzy functions as in the following.

Rule A: (if the cloth quantity is medium, water current is medium)

Rule B: (if the cloth type is stiff, water current is strong)

As shown in FIG. 9, a water current Fuzzy function (A3) is obtained based on Rule A, and a water current Fuzzy function (B3) is obtained based on Rule B. The two functions are composed, and the center of gravity of this composite Fuzzy function is calculated by the microcomputer and becomes an optimum motor on-time which is used during washing

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RTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2022 – 2023 (ODD SEMESTER)

STUDENTS MARK STATEMENT- CO BASED

INTERNAL ASSESSMENT-I

SUBJECT CODE &TITLE: AP5191 EMBEDDED SYSTEM DESIGN

YEAR/SEM: I/II **MONTH & YEAR: Feb 2019**

S.NO	REG NO	STUDENT NAME	CO1	Retest CO1	TOTAL (100)
1.	811218419002	Shalini K	36	-	72
2.	811218419003	Velrajeswari M R	41	-	82

MARKS RANGE:

<20	20-30	31-40	41-50	51-60	61-70	71-80	81-90	91-100
0	0	0	0	0	0	1	1	0

Total No.of Candidates Present	2
Total No.of Candidates Absent	Nil
Total No.of Students Pass	2
Total No. of Students Fail	0
Percentage of Pass	100 %

STAFF INCHARGE HoD/ECE PRINCIPAL

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Assignment Questions

Assignment – 01			Date of Issue:	02.02.2019	Marks	10
Course code	AP5191	Course Title	Embedded System Design			
Year	I	Semester/Section	II/ A	Date of Submission:	08.02.2019	

Q.No	Questions	CO
1.	Design methodology for Model train controller.	C113.1
2.	Write an Detail notes on RT level Combinational Circuit.	C113.1
3.	Write an Detail notes on RT level Sequential Circuit.	C113.1

Name and Signature of the Faculty Incharge

HoD/ECE

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Assignment Answer Sheet

Name of the Student : Vel Rajeswari

AU Register Number: 811218419003

Assignment – 01			Date of Issue:	02.02.2019	Marks	10
Course code	AP5191	Course Title	Embedded System Design			
Year	I	Semester/Section	II/ A	Date of Submission:	08.02.2019	

Q.No	Questions	CO
1.	Design metodology for Model train controller.	C113.1
2.	Write an Detail notes on RT level Combinational Circuit.	C113.1
3.	Write an Detail notes on RT level Sequential Circuit.	C113.1

Mark Allocation

Rubrics	Marks Allocated	Marks obtained
Content Quality	**6**	**6**
Presentation Quality	**2**	**2**
Timely submission	**2**	**2**
Total marks	**10**	**10**

Name and Signature of the Faculty Incharge

K. Kuman.

HoD/ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

Register Number:

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India

(Approved by AICTE, New Delhi and affiliated to Anna University, Chennai)

Internal Assessment Exam - I			Date/Session	06.02.19/FN	Marks	50
Course code	AP5191	Course Title	EMBEDDED SYSTEM DESIGN			
Regulation	2017	Duration	90 minutes	Academic Year	20 -18-2019	
Year	I	Semester	II	Department	ME –VLSI Design	

COURSE OUTCOMES

CO1:	Function of the Architecture of 8086 microprocessor.
CO2:	Learn the design aspects of I/O and Memory Interfacing circuits.
CO3:	Interface microprocessors with supporting chips.
CO4:	Study the Architecture of 8051 microcontroller
CO5:	Design a microcontroller based system
CO6:	Study the Advanced Processors

Q.No.	Question	CO	BTS
	PART A (Answer all the Questions 9 x 2 = 18 Marks)		
1	What is an Embedded computer system?	CO1	K1
2	What is an Embedded computer system?	CO1	K4
3	Formulate the importance of design methodology.	CO1	K2
4	Describe the major steps in embedded system design process.	CO1	K1
5	Categories the steps involved in system analysis using CRC card.	CO1	K2
6	Can you elaborate, Quality Assurance Techniques?	CO1	K2
7	What are the services to be provided by consumer electronics?	CO1	K3
8	Illustrate the three different profiles of ARM cortex Processor	CO1	K1
9	Evaluate the important features that make ARM ideal for embedded applications.	CO1	K3
10	Name the registers set of ARM processor		
	PART B (Answer all the Questions 2 x 14 = 28 Marks)		
11a	(i)Mention the requirements for designing a GPS moving map in embedded system design process.(7) (ii)Write down the major operations and data flows of a GPS moving map and draw its Architecture. (3)	CO1	K3
	OR		
11b	Design in detail a Model Train Controller with suitable diagrams.(7) (ii)Formulate design steps of Model Train Controller in detail. (3)	CO1	K3
12a	From the fundamentals, draw the architecture of ARM processor with relevant explanation.	CO1	K3
	OR		
12b	Explain in detail about in data processing and branching instruction	CO1	K3
	PART C (Answer all the Questions 1 x 14 = 14 Marks)		
13a	Write short note on the following in terms of consumer electronics system architecture(i)Use Cases and Requirements,(ii)Platforms and Operating Systems,Flash File Systems. (10)	CO2	K3
	OR		
13b	Design in detail with computing platforms.	CO2	K3

Course Faculty
(Name /Sign / Date)
k. kumar 04/2/19

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HoD
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STUDENT FEEDBACK ON FACULTY

THEORY COURSE

ACADEMIC YEAR: 2018-2019 EVEN SEMESTER

Name of Department :	ME	Year / Sem:	I / II	Faculty Name	Mr.K.Kumar
Subject Code & Name	AP5191 EMBEDDED SYSTEM DESIGN				

S.No.	QUESTIONS	Excellent	Very Good	good	Satisfactory	Somewhat Satisfactory	Not Satisfactory
		5	4	3	2	1	0
1.	Delivery of Lectures by Interactive Communication	2	0	0	0	0	0
2.	Use of Teaching Aids and ICT	1	1	0	0	0	0
3.	Level of Preparedness & Knowledge Level	-	2	0	0	0	0
4.	Involvement in mentoring and guiding	1	1	0	0	0	0
5.	Effective Time management	-	2	0	0	0	0
6.	Is the teacher completing syllabus as per lecture schedule?	2	0	0	0	0	0
7.	Is the teacher distributing answer scripts of students as per schedule?	-	2	0	0	0	0
8.	Is the teacher addressing grievances on answer scripts of IA while distributing?	2	0	0	0	0	0
9.	Is the teacher covering content beyond syllabus (CBS)?	-	2	0	0	0	0
10.	Is the teacher punctual to class?	-	2	0	0	0	0

HoD/ ECE

Principal

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