

Accredited by NAAC with 'B+' Grade, 2(f) & 12B Status Institution by UGC

IG Valley, Madurai Main Road, Manikandam, Tiruchirappalli - 620012

NAAC DOCUMENTS

QUALITY INDICATOR FRAME WORK

CRITERION – 1

CURRICULAR ASPECTS

SUBMITTED BY

IQAC

INTERNAL QUALITY ASSURANCE CELL INDRA GANESAN COLLEGE OF ENGINEERING





Citteria i	Criteria 1	Curricular Aspects	100
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1.1 Curricular Planning and Implementation (20)

1.1.1 The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment

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IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India (Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF INFORMATION TECHNOLOGHY

PREFACE OF THE COURSE FILE

Batch

: 2019-2023

Academic Year

: 2020-2021 / EVEN

Program

: INFORMATION TECHNOLOGHY

Year & Semester

: 2rd Year / IVth Semester

Course Code

: CS8491

Name of the Course

: Computer Architecture

Faculty in-charge

: Mrs. S. Saroja Devi

Signature of the Faculty in-charge

HoD/IT



COLLEGE CIFENCIINE EXTINES Name of the STAIN CONTRACTOR Name (NH-458), Manikandom, Truchirapelli 620 012
Approved by AlCTE, NewDelhi & Affiliated to Anna University, Chennal Accredited by NAAC with B+Grade

DEPARTMENT OF INFORMATION TECHNOLOGY

Academic Year 2020-2021 (Even Semester)

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Time Table Co-ordinator

Dr. G. Balakrishnan, M.E., Ph.D., Principal

	Class: II Year / IV Sem	Sem	Manager Springer	hibitahona nast			מבווו	ialsar		,	TRACOON	
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Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

Signature of the Faculty

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DEPARTMENT OF INFORMATION TECHNOLOGHY

CS8491

COMPUTER ARCHITECTURE

LTPC 3003

OBJECTIVES:

- To learn the basic structure and operations of a computer.
- To learn the arithmetic and logic unit and implementation of fixed-point and floating point arithmetic unit.
- To learn the basics of pipelined execution.
- To understand parallelism and multi-core processors.
- To understand the memory hierarchies, cache memories and virtual memories.
- To learn the different ways of communication with I/O devices.

UNIT I BASIC STRUCTURE OF A COMPUTER SYSTEM 9

Functional Units – Basic Operational Concepts – Performance – Instructions: Language of the Computer – Operations, Operands – Instruction representation – Logical operations – decision making – MIPS Addressing.

UNIT II ARITHMETIC FOR COMPUTERS

Addition and Subtraction – Multiplication – Division – Floating Point Representation – Floating Point Operations – Subword Parallelism

UNIT III PROCESSOR AND CONTROL UNIT

A Basic MIPS implementation – Building a Datapath – Control Implementation Scheme – Pipelining – Pipelined datapath and control – Handling Data Hazards & Control Hazards – Exceptions.

UNITIV PARALLELISIM 9

Parallel processing challenges – Flynn's classification – SISD, MIMD, SIMD, SPMD, and Vector Architectures - Hardware multithreading – Multi-core processors and other Shared Memory Multiprocessors - Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message-Passing Multiprocessors.

UNIT V MEMORY & I/O SYSTEMS 9

Memory Hierarchy - memory technologies - cache memory - measuring and improving cache performance - virtual memory, TLB's - Accessing I/O Devices - Interrupts - Direct Memory Access - Bus structure - Bus operation - Arbitration - Interface circuits - USB.

TOTAL: 45

PERIODS OUTCOMES:

On Completion of the course, the students should be able to: Understand the basics structure of computers, operations and instructions.

- Design arithmetic and logic unit.
- Understand pipelined execution and design control unit.
- Understand parallel processing architectures.
- Understand the various memory systems and I/O communication.

TEXT BOOKS:

1. David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Fifth Edition, Morgan Kaufmann / Elsevier, 2014.

Dr. G. Balakrishnan, M.E., Ph.D.,

Principal

2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky and Naraig Manjikian, Computer Organization and Embedded Systems, Sixth Edition, Tata McGraw Hill, 2012.

REFERENCES:

- 1. William Stallings, Computer Organization and Architecture Designing for Performance, Eighth Edition, Pearson Education, 2010.
- 2. John P. Hayes, Computer Architecture and Organization, Third Edition, Tata McGraw Hill, 2012.
- 3. John L. Hennessey and David A. Patterson, Computer Architecture A Quantitative Approachl, Morgan Kaufmann / Elsevier Publishers, Fifth Edition, 2012.

Hod/IT

PRINCIPAL

Dr. G. Balakrishnan, M.E., Ph.D.,

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India (Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF INFORMATION TECHNOLOGHY

Ref: SBECW/ IT / Course committee meeting / EM-I/ 2020-21 (Even)

DATE: 21.01.2021

COURSE COMMITTEE MEETING-CS8491-COMPUTER ARCHITECTURE

ACADEMIC YEAR: 2020-2021 (EVEN) SEM: 04

REGULATION: 2017

PROGRAM: IT

DATE OF MEETING: 21.01.21 TIME: 10.00AM

Venue: IT Dept. HoD Cabin

Members Present

Table.1 Course committee members

S.No.	Name of the faculty & Designation, Program	Sem/Sec/Program	Signature
1.	Dr.K. Uthradevi ASP/IT - Course coordinator	IV SEM/IT	wilable as parentiment monormic lang Aphibit
2.	Mr. A. Vivek Ignatius	IV SEM// IT	promanagagago, and Williamster, los as a second and another real

HOD welcomed all the members present

- 1. Content of syllabus, unit wise discussed. Nature of qualitative, quantitative, problematic, theoretical concepts etc. have been discussed
- 2. With reference to the R-2017 regulation, Number of periods per unit = 09, total number of periods = 45 periods. 10 periods allotted for tutorials.
- 3. Vision and mission of the college, department discussed. POs, PEOs, PSOs discussed.
- 4. Course outcomes defined for each units, considering learning outcomes.

Table.2 Course Outcomes CO Course Outcomes **PSOs** C202.1 Understand the basics structure of computers, operations and 1,2,3,4,5,6,7,8,9,10,11,12 1,2 instructions. C202.2 Design arithmetic and logic unit. 1,2,3,4,5,6,7,8,9,10,11,12 1.2 C202.3 Understand pipelined execution and design control unit. 1,2,3,4,5,6,7,8,9,10,11,12 1,2 C202.4 Understand parallel processing architectures. 1,2,3,4,5,6,7,8,9,10,11,12 1.2 C202.5 Understand 1,2,3,4,5,6,7,8,9,10,11,12 1.2 the various 1/0 memory systems and communication

5. Mapping of COs with POs and PSOs is done with suitable correlation levels(1 for low, 2 for medium, 3 for high, "-" for no correlation, before content beyond syllabus)

Table.3 Mapping of COs, C, PSOs with POs-before CBS.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C202.1	3	2	3		2	2	2	-		3	-	2	2	2
C202.2	3	-	3	2		2	2		2			2	2	2
C202.3	3	-	3	- 40-40-0-0	•	2	2	-	-	- 1	2	2	2	2
C202.4	3	2	3	2	2	2	. ,		2	-	**	2	2	2
C202.5		-			46	2	2		i handware a	3	2	2	2	2

6. Identification of content beyond syllabus- curricular gaps are identified considering industry needs, employers feedback, alumni feedback, government policy on industrialization, new investments by private/public sectors, societal needs and level of correlation of COs with POs and PSOs. Accordingly the details of CBS added and its correlation is given below.

Dr. G. Balakrishnan, M.E., Ph.D.,

Principal

Table 4 Identification of content beyond syllabus

Content beyond syllabus added	POs strengthened/Vacant filled	
Communication Components	PO9 Vaccant Filled	C302.3 & C302.5/III & V

7. Mapping of COs with POs, PSOs- after CBS.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	POII	PO12	PSO1	PSO2
C202.1	3	2	3	-	2	2	2	-	-	3		2	2	2
C202.2	3		3	2	-	2	2	-	2	-	-	2	2	2
C202.3	3	-	3	**	-	2	2	-	2	-	2	2	2	2
C202.4	3	2	3	2	2	2	-	-	2	•	-	2	2	2
C202.5		-	-	-		2	2	_	2	3	2	2	2	2

- 8. Content beyond syllabus is thus identified based on the above. Plan for handling of CBS by internal/external resource person/ industrial visits are decided. This will be included in the class log book.
- 9. Lecture schedule should be prepared unit wise, as in the syllabus. Number of periods per unit and total number of periods planned should not be less than, periods allotted in the syllabus of Anna University.
- 10. Plan for additional Periods for IA tests, CBS, NPTEL delivery, Seminar, Quiz etc are to be incorporated in the lecture schedule. These periods are added exclusive of number of periods prescribed in the syllabus.
- 11. Plan for at least three assignments (with level of correlation), seminar topic, quiz questions discussed.
- 12. Separate tutorial sheets should be prepared and supplied to all students. Minimum two periods per unit to be planned, totally 10 tutorial periods. Minimum 2 tutorial questions should be set per unit, totally 10 tutorial questions.
- 13. Bright students and slow learners are to be identified, immediately after IA test I. such students may be counselled suitably and the evidence for counselling to be recorded in the attendance cum assessment record. (Sign of students with date and time of counselling, to be strictly recorded and to be attached in the course file). Such counselling may be conducted after college hours.
- 14. For those students secured less than 60% in the IA Test, Makeup test should be conducted. Correspondingly root cause analysis for reasons of failure, corrective and preventive action, and follow up action taken should be filed properly.
- 15. Contents of course file to be reviewed periodically.
- 16. Lecture schedule, assignment questions, tutorial questions, course materials, AU questions (at least 5) should be supplied within one week after the commencement of classes.
- 17. Course material should be uploaded in the college website for student's reference.
- 18. Discrepancy in question paper, if any to be informed to the controller of examinations through web portal entry, after getting approval from the HoD & the Principal. Critically asked questions, if any to be discussed with the students of the next batch.
- 19. Immediately after the publication of the results, analysis are to be carried out and follow up action to be taken for the failures.
- 20. IA test question papers should be set as per the norms of the college, incorporating marks for learning outcomes and course outcomes. Common question papers should be set.
- 21. Certificate courses/Workshop/guest lectures may be planned inviting experts from industry/higher learning institutions.
- 22. After IA test, an objective type tests may be conducted (3 times in a semester-30 minutes duration-maximum 10 questions). Questions asked in GATE, TANCET, IES or any other Competitive examination can be taken as a reference. This is to facilitate the bright students to prepare for higher level of thinking and to enhance placement and higher studies opportunities.
- 23. IA test papers, assignment papers or any other papers submitted by the students, should be returned to the students within 5 days after correction. Sample paper should be suitably filed.
- 24. Long absentees of students if any to be informed to the parents through class coordinator, if such students attendance less than 75%.

Course coordinator

HoD/IT

Dr. G. Balakrishnan, M.E., Ph.D.,

Principal

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu - 620 012, India (Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF INFORMATION TECHNOLOGHY

Lecture Schedule

Degree/Program: B.TECH / IT

Regution: 2017

Course code &Name: CS8491 & CA

Semester: IV Faculty: Mrs.S. Saroja Devi

AIM:

To expose the students to principle of operation and performance of electrical machines **OBJECTIVES:**

To impart knowledge on

To learn the basic structure and operations of a computer.

- To learn the arithmetic and logic unit and implementation of fixed-point and floating point arithmetic unit.
- To learn the basics of pipelined execution.
- To understand parallelism and multi-core processors.
- To understand the memory hierarchies, cache memories and virtual memories.
- To learn the different ways of communication with I/O devices..

PREREOUISITIES:

Circuit theory, Electromagnetic theory.

COURSE OUTCOMES:

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C402.1	Understand the basics structure of computers, operations and instructions.	1,2,3,4,5,6,7,8,9,10,11,12	1,2
C402.2	Design arithmetic and logic unit.	1,2,3,4,5,6,7,8,9,10,11,12	1,2
C402.3	Understand pipelined execution and design control unit.	1,2,3,4,5,6,7,8,9,10,11,12	1,2
C402.4	Understand parallel processing architectures.	1,2,3,4,5,6,7,8,9,10,11,12	1,2
C402.5	Understand the various memory systems and I/O communication	1,2,3,4,5,6,7,8,9,10,11,12	1,2

Dr. G. Balakrishnan, M.E., Ph.D.,

S.No	Date	Topics to be Covered	Book
	a here you		Target periods :09
1	6.2.21	Functional Units	
2	7.2.2	Basic Operational Concepts	
3	7.2.21	Performance	And the same of th
4	8.2.21	Instructions: Language of the Computer	
5	9.2.21	Operations, Operands	
6	10.2.21	Instruction representation	Online
7	15.2.21	Logical operations	NAME OF THE PARTY
8	16.2.21	decision making	
9	17.2.21	MIPS Addressing	
10	21.2.21	Tutorial	
11	21.2.21	Tutorial	
UNIT	II - ARITH	IMETIC FOR COMPUTERS	Target periods :09
12	28.2.21	Addition and Subtraction	Online
13	01.3.21	Multiplication	AND POST OF TOTAL PROCESS AND
14	3.3.21	Division	 In departure production of the contract of the co
15	16.3.21	Floating Point Representation	the account of the second party in the second
16	20.3.21	Floating Point Representation	ninga ngangan midika kang ding kang kang kang kang kang kang kang ka
17	21.3.21	Floating Point Operations	as a halah dasada karanta yang bahasa makka nada da
18	24.3.21	Floating Point Operations	y 442 Aug
19	27.3.21	Subword Parallelism	
20	27.3.21	Subword Parallelism	
21	28.3.21	Tutorial	200
22	28.3.21	Tutorial	weather the executificate lands
JNIT	III -PROCE	SSOR AND CONTROL UNIT	Target Periods :09
23	30.3.21	A Basic MIPS implementation	Online
24	31.3.21	Building a Datapath	and the same of th
25	3.4.21	Control Implementation Scheme	Approximation Approximation (Control of Control of Cont
26	5.4.21	Pipelining	APPER PRE PRESENTAL ALL APPERS PROCESSAR (POST SERVICES AS A SERVICE AS A SERVICES AS A SERVICE AS A SER
27	6.4.21	Pipelined datapath and control	a parties are sidentes de la constante de la c
28	10.4.21	Handling Data Hazards & Control Hazards	1
39		Handling Data Hazards & Control Hazards	
-		Exceptions.	noted throughous as con-
	appropriate on their land of the	Tutorial	- MANAGE - MANAGE AND
detressesses		Tutorial	Exercise hour administrating promptings
NIT I	V - PAF	RALLELISIM	Target Periods :09
33	26.4.21	Parallel processing challenges	Online
	28.4.21	-	- Cililli
netr Comm		Flynn's classification	fi. appropriate and appropriat
36	v	SISD, MIMD, SIMD, SPMD, and Vector Architectures	and or real additional for souther sequences dated
37		Hardware multithreading	alacida da Mara Picciona, ana cana anterior anterior de montra de la companya del companya de la companya de la companya del companya de la c
38	4.5.21	attan a trianglin anality	
39	-	Multi-core processors and other Shared Memory Multiprocessors	

40	10.5.21	ntroduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message	
41	10.5.21	Passing Multiprocessors.	Add Add Add Add age a sum and
42	12.5.21	Tutorial	a considerate de la mandada de
UNIT	V- MEM	IORY & I/O SYSTEMS	Target Periods:09
43	12.5.21	Memory Hierarchy	Online
44	15.5.21	memory technologies	
45	15.5.21	cache memory	
46	16.5.21	measuring and improving cache performance	
47	16.5.21	- virtual memory, TLB's	
48	17.5.21	Accessing I/O Devices	
49	17.5.21	Interrupts	a acedia
50	18.5.21	Direct Memory Access, Bus structure	-
51	18.5.21	Bus operation, Arbitration, Interface circuits, USB.	yada aa'aa a (497-a
52		Tutorial	
53		Tutorial	
	aba	Content Beyond the Syllabus	udgestatengi salammany. Kal-11 z
54		Communication Component's	Online

Book Reference - Text Books

SI.	Title of the Book	Author	Publisher	Year
que .	Computer Organization and Design The Hardware/Software Interface,	David A. Patterson and John L. Hennessy,	Fifth Edition, Morgan Kaufmann / Elsevier	2014
2.	Computer Organization and Embedded Systems	. Carl Hamacher, Zvonko Vranesic, Safwat Zaky and Naraig Manjikian,	Sixth Edition, Tata McGraw Hill	2012

(D).

Sl. No	Title of the Book	Author	Publisher	Year
1	Computer Organization and Architecture – Designing for Performance	William Stallings	Pearson Education	2010

Signature of the Paculty in-charge

HoD/IT

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India (Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF INFORMATION TECHNOLOGHY

Identification of Curricular Gap & Content Beyond Syllabus(CBS)

Name of the Faculty: Mrs. S. Saroja Devi

Course Code & Name: CS8491 & CA

Technology Degree & Program: B.TECH/IT

Semester: IV Year: 2020 -2021 /EVEN

I.Mapping of Course Outcomes with POs & PSOs.(before CBS)

Table 1 Mapping of COs. C. PSOs with POs - before CBS.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C202.1	3	2	3	-	2	2	2	-	_	3	no so narridge de fração	2	2	2
C202.2	3	-	3	2	200	2	2	***	2	***	-	2	2	2
C202.3	3	-	3	-	-	2	2		_	-	2	2	2	2
C202.4	3	2	3	2	2	2	-		2	- 1	-	2	2	2
C202.5		-	***	_	- 1	2	2	_		3	2	2	2	2
C202	3 ;	3	3 .	2	3	2	2	-	7	3	2	7	2	3

II. Identification of content beyond syllabus.

Table.2 Identification of content beyond syllabus

Details of Content Beyond Syllabus(CBS) added	POs strengthened/ vacant filled	CO/Unit
Communication Communication	PO9	C202.3 & III
Communication Components	(Vacant	
	filled	

III. Mapping of Course Outcomes with POs & PSOs. (After CBS)

Table.3 Mapping of COs, C, PSOs with POs- after CBS.

Course	PO 1	PO2	PO3	PO4	PO5		PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C202.1	3	2	3	-	2	2	2	-	-	3	-	2	2	2
C202.2	3	-	3	2	-	2	2	-	2	-	-	2	2	2
C202.3	3	MAR.	3	жо	-	2	2	_	*2	-	2	2	2	2
C202.4	3	2	3	2	2	2	-		2		-	2	2	2
C202.5	-	ine .	***	-	-	2	2	w	*2	3	2	2	2	2
C202	3	2	3	2	2	2	2	-	7	3	2	2	2	2

Signature of the Faculty

0:

HoD/ IT

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu - 620 012, India (Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF INFORMATION TECHNOLOGHY

Proof and identification of Content Beyond Syllabus(CBS)

Name of the Faculty: Mrs. S. Saroja Devi

Course Code & Name: CS8491 & CA

Degree & Program: B.TECH & IT

Semester: IV Academic Year: 2020 -2021 /EVEN

TOPIC: Communication Components

Components of Computer Architecture

Depending on the method of categorization, the parts of a computer architecture can be subdivided in several ways. The main components of a computer architecture are the CPU, memory, and peripherals. All these elements are linked by the system bus, which comprises an address bus, a data bus, and a control bus. Within this framework, the computer architecture has eight key components, as described below.

Components of Computer Architecture

Input unit and associated peripherals



Output unit and associated peripherals



Storage unit/memory

Central processing unit (CPU)

Operating system (OS)

spiceworks

Components of Computer Architecture

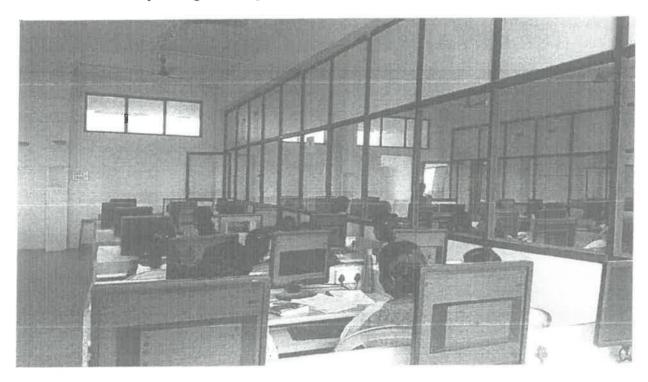
1. Input unit and associated peripherals

The input unit provides external data sources to the computer system. Therefore, it connects the external environment to the computer. It receives information from input devices, translates it to machine language, and then inserts it within the computer system. The keyboard, mouse, or other input devices are the most often utilized and have corresponding <u>hardware drivers</u> that allow them to work in sync with the rest of the computer architecture.

2. Output unit and associated peripherals

The output unit delivers the computer process's results to the user. A majority of the output data comprises music, graphics, or video. Computer architecture's output devices encompass the display, printing unit, speakers, headphones, etc.

To play an MP3 file, for instance, the system reads a number array from the disc and into memory. The computer architecture manipulates these numbers to convert compressed audio data to uncompressed audio data and then outputs the resulting set of numbers (uncompressed audio file) to the audio chips. The chip then makes it user-ready through the output unit and associated peripherals.



Signature of the Culty

HOD/IT

Dr. G. Balakrishnan, M.E., Ph.D.,

Principal

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India (Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF INFORMATION TECHNOLOGHY

Assignment Question Paper

	Assignmen	ıt — 01	Date of Issue:	12.03.2021	Marks	10
Course code	CS8491	Course Title	Computer Archite	cture		
Year	11	Semester	IV	Date of Submission:	18.03.202	21

Q.No	Questions	CO
1	Subword Parallelism	C202.3
2	Handling Data Hazards & Control Hazards – Exceptions	C202.3

Mark Allocation

Rubrics	Marks Allocated	Marks obtained
Content Quality	6	5
Presentation Quality	2	2
Timely submission	2	2
Total marks	10	9

Name and Signature of the Faculty In-charge

HoD/IT

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India (Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF INFORMATION TECHNOLOGHY

Tutorial Ouestion Paper

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Course code	CS8491	Course Title	Computer Archite	ecture	
Year	II	Semester	IV	Date of Submission:	26 .04.2021

Q.No	Questions	CO
1	Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message	C202.4
2	Flynn's classification	C202.4

Name and Signature of the Faculty In-charge

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HoD/IT



GOLLEGE OF ENGINEERING Approved by AlCTE, New John Warn Road (NH-45B), Manikandam, Truchinappalli - 620 012 Approved by AlCTE, New John Anna University, Cheminal Manikandam, 2(P) Status Joseft utolon by UGC



Internal Assessment Test - I Even Sem Time Table (Higher Semester) - 2020-21

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Dr. G. Balakrishnan, M.E., Ph.D.,



Register Number:



INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India (Approved by AICTE, New Delhi and affiliated to Anna University, Chennai)

	Internal Assessi	nent Exam - I	Date/Session	18.04.2021 M	arks 50					
Course	code CS8491	Course Title	Computer Architecture							
Regulat	ion 2017	Duration	90 minutes Academic Year		2020-2021					
Year	11	Semester	IV	Department	IT					
COURS	E OUTCOMES	Broom or control of the control of t	EVEL THE	The second second second						
CO1:	To learn the basic str	ucture and operations of a	computer	*** **********************************	more and additionally pulled in a laborate and abilitial income					
CO2:	To learn the arithmet	ic and logic unit and imple	ementation of fixed-n	oint and floating moint	arithmetic unit					
CO3:	To learn the basics of	f pipelined execution.	The state of the s	ome and moaning point	artiffictic unit.					
CO4:	To understand parall	elism and multi-core proce	escors	ini dipendanyan sacross sassandara s. 1496 18.						
CO5:	To understand the memory hierarchies, cache memories and virtual memories.									
CO6: To learn the different ways of communication with I/O devices.										

Q.No.	Question	СО	BTS
	PART A (Answer all the Questions 10 x 2 = 20 Marks)		Morton
1	What are the components of a computer system?	CO1	K1
2	Give the formula for CPU execution time for a program.	CO1	K2
3	Define Program Counter.	CO1	K2
4	How to represent instruction in a computer system?	COI	K1
5	State the needs of indirect addressing mode. Give Example.	CO1	K1
6	What do you mean by zero address instruction?	COI	K1
7	Brief about relative addressing mode with an example.	COI	K3
8	Subtract(11010) ₂ -(10000) ₂ using 2's complement method.	CO2	
9	Draw the Half-adder circuit.		K2
10	Write the rule for addition of two binary numbers.	CO2	K5 K2
11a	i. Explain the functional units of a computer in detail. ii. Write note on various types of registers. OR	COI	K6
11b	Explain the various instruction formats with example.	CO1	K6
12a	Design a full-adder circuit and explain in detail	CO2	er-e
THE SECTION SHEET	OR	CUZ	K2
12b	Explain the Multiplication operation using flowchart and Multiply B=1101 and Q=1011 using the process	CO2	K2
diharangaya	PART C (Answer all the Questions 1 x 10 = 10 Marks)		
3a	Draw a neat sketch, explain in detail about logic design for carry look-ahead adder	COI	K2
-	OR	Amendon of	
3b	Classify MIPS addressing Modes and give examples for each.	COI	K2
		netho	****************

Course Faculty

(Name/Sign/Date)

HoD

(Name /Sign / Date)

Dr. G. Balakrishnan, M.E., Ph.D.,



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Medural Main Road (NH-45B), Manikandam, Thuchinappali - 820 012
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Branch	YEAR	1.03.21	2.03,21	3.03.21	4.03.21	5.03.21	6.03.71
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Dr. G. Balakrishnan, M.E., Ph.D., Indra Ganesan College of Engineering ान Valley, Madurai Main Roहर् Randam, Trichy-620 012. Principal



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IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 622 012, India (Approved by AICTE, New Delhi and affiliated to Anna University, Chennai)

Internal Assessment Test Answer Book

Name	Tamil S	elvi. T		ection	12/	15			
Batch No.	2020 - 2021	Date/Session	23.2.21 FN	Department		IT	a m. worklin to		
Course code	CS 8491	Course Title	Computer Architecture						
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IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India (Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

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Dr. G. Balakrishnan, M.E., Ph.D., Principal

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India (Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF INFORMATION TECHNOLOGHY

ROOT CAUSE ANALYSIS

Name of the Faculty: S. Sareja Devi

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Signature of the Faculty

Dr. G. Balakrishnan, M.E., Ph.D.,

Principal Indra Ganesan College of Engineering IG Valley, Madurai Main Road Manikandam, Trichy-620 012.

Signature of the HOD/ IT