Indra Ganesan
COLLEGE OF ENGINEERING

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai
Accredited by NAAC with 'B+' Grade, 2(f) & 12B Status Institution by UGC
IG Valley, Madurai Main Road, Manikandam, Tiruchirappalli - 620012

NAAC DOCUMENTS

QUALITY INDICATOR FRAME WORK

CRITERION – 1

CURRICULAR ASPECTS

SUBMITTED BY

IQAC

INTERNAL QUALITY ASSURANCE CELL

INDRA GANESAN COLLEGE OF ENGINEERING

Criteria 1	Curricular Aspects	100

1.1 Curricular Planning and Implementation (20)

1.1.1 The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment

Table of Content

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF INFORMATION TECHNOLOGHY

PREFACE OF THE COURSE FILE

Batch	: **2019-2023**
Academic Year	: **2020-2021 / EVEN**
Program	: **INFORMATION TECHNOLOGHY**
Year & Semester	: **2rd Year / IVth Semester**
Course Code	: CS8491
Name of the Course	: **Computer Architecture**
Faculty in-charge	: Mrs. S. Saroja Devi

Signature of the Faculty in-charge

HoD/IT

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

Indra Ganesan
COLLEGE OF ENGINEERING

Madurai Main Road (NH-45B),Manikandam,Tiruchirapalli- 620 012
Approved by AICTE, NewDelhi & Affiliated to Anna University, Chennai
Accredited by NAAC with B+ Grade

DEPARTMENT OF INFORMATION TECHNOLOGY

Academic Year 2020-2021 (Even Semester)

Class: II Year / IV Sem — **Class Coordinator: Mr. S. Saroja Devi**

Day	1	2	BREAK	3	4	LUNCH	5	6	BREAK	7	SCC/ CCA
	9.15 - 10.10	10.10- 11.00		11.10-12.00	12.00-12.48		1.45-2.30	2.30-3.15		3.30 - 4.10	4.10 - 5.00
MON	DBMS	DAA		EVS	PS		EVS	CA		OS	DBMS/KN
TUE	CA	DAA		ARW			OS	DBMS		PS	PS/KUD
WED	EVS	DBMS		DAA	DBMS LAB		DBMS LAB			DBMS LAB	EVS/SSD
THUR	OS	PS		DAA	OS LAB		OS LAB			OS LAB	DAA/NS
FRI	DBMS	CA		PS	CA		EVS	OS		PS	OS/BP

SUBJECT CODE	COURSE NAME	ERP ID	CREDITS/ HOURS	STAFF IN-CHARGE
MA8391	Probability & Statistics		4/ 60	E. Sujana AP/Maths
CS8491	Computer Architecture		3/ 45	S. Saroja Devi AP/ IT
CS8492	Database Management Systems		3/ 45	M. Karthiga AP/ IT
CS8451	Design and Analysis of algorithms		3/ 45	K. Uthra Devi AP/IT
CS8493	Operating Systems		3/ 45	S. Jenila AP/IT
GE8291	Environmental Science and Engineering		2/ 60	A. Ramya AP
CS8481	Database Management Systems Laboratory		2/ 60	M. Karthiga AP/ IT
CS8461	Operating Systems Laboratory		2/ 60	S. Jenila AP/IT
HS8461	Advanced Reading and Writing		1/ 30	F. Maria Kiruba Priyadharshini AP/English

Time Table Co-ordinator

HOD/ IT

Dr. G. Balakrishnan, M.E., Ph.D.,
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Indra Ganesan College of Engineering
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Manikandam, Trichy-620 012.

DEPARTMENT OF INFORMATION TECHNOLOGY

Academic Year 2020-2021 (Even Semester)

Class: II Year / IV Sem — **Class Coordinator: Mrs. S. Saroja Devi**

Day	TEST 9.15 - 10.00	1 10.00 - 10.45	BREAK	2 11.00 - 11.45	3 11.45 - 12.30	4 12.30 - 1.15	LUNCH	5 2.00 - 2.45	6 2.45 - 3.25	BREAK	7 3.35 - 4.15	8 4.15 - 5.00
MON									CA			
TUE	CA											
WED												
THUR												
FRI				CA		CA		Professional Communication				

S.Code	Title	Year/Branch	Hours
CS8491	Computer Architecture	II / IT	4

Signature of the Faculty

Dr. G. Balakrishnan, M.E., Ph.D.,
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HOD/IT

INDRA GANESAN COLLEGE OF ENGINEERING

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DEPARTMENT OF INFORMATION TECHNOLOGHY

CS8491 COMPUTER ARCHITECTURE **L T P C**
3 0 0 3

OBJECTIVES:

- To learn the basic structure and operations of a computer.
- To learn the arithmetic and logic unit and implementation of fixed-point and floating point arithmetic unit.
- To learn the basics of pipelined execution.
- To understand parallelism and multi-core processors.
- To understand the memory hierarchies, cache memories and virtual memories.
- To learn the different ways of communication with I/O devices.

UNIT I BASIC STRUCTURE OF A COMPUTER SYSTEM 9

Functional Units – Basic Operational Concepts – Performance – Instructions: Language of the Computer – Operations, Operands – Instruction representation – Logical operations – decision making – MIPS Addressing.

UNIT II ARITHMETIC FOR COMPUTERS 9

Addition and Subtraction – Multiplication – Division – Floating Point Representation – Floating Point Operations – Subword Parallelism

UNIT III PROCESSOR AND CONTROL UNIT 9

A Basic MIPS implementation – Building a Datapath – Control Implementation Scheme – Pipelining – Pipelined datapath and control – Handling Data Hazards & Control Hazards – Exceptions.

UNIT IV PARALLELISIM 9

Parallel processing challenges – Flynn's classification – SISD, MIMD, SIMD, SPMD, and Vector Architectures - Hardware multithreading – Multi-core processors and other Shared Memory Multiprocessors - Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message-Passing Multiprocessors.

UNIT V MEMORY & I/O SYSTEMS 9

Memory Hierarchy - memory technologies – cache memory – measuring and improving cache performance – virtual memory, TLB's – Accessing I/O Devices – Interrupts – Direct Memory Access – Bus structure – Bus operation – Arbitration – Interface circuits - USB.

TOTAL : 45

PERIODS OUTCOMES:

On Completion of the course, the students should be able to: Understand the basics structure of computers, operations and instructions.

- Design arithmetic and logic unit.
- Understand pipelined execution and design control unit.
- Understand parallel processing architectures.
- Understand the various memory systems and I/O communication.

TEXT BOOKS:

1. David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Fifth Edition, Morgan Kaufmann / Elsevier, 2014.

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2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky and Naraig Manjikian, Computer Organization and Embedded Systems, Sixth Edition, Tata McGraw Hill, 2012.

REFERENCES:

1. William Stallings, Computer Organization and Architecture – Designing for Performance, Eighth Edition, Pearson Education, 2010.

2. John P. Hayes, Computer Architecture and Organization, Third Edition, Tata McGraw Hill, 2012.

3. John L. Hennessey and David A. Patterson, Computer Architecture – A Quantitative Approachl, Morgan Kaufmann / Elsevier Publishers, Fifth Edition, 2012.

Hod/IT

PRINCIPAL

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DEPARTMENT OF INFORMATION TECHNOLOGHY

Ref: SBECW/ IT / Course committee meeting / EM-I/ 2020-21 (Even) DATE: 21.01.2021

COURSE COMMITTEE MEETING-CS8491-COMPUTER ARCHITECTURE

ACADEMIC YEAR: 2020-2021 (EVEN) **SEM:** 04 **REGULATION:** 2017
PROGRAM: IT **DATE OF MEETING:** 21.01.21 **TIME:** 10.00AM **Venue:** IT Dept. HoD Cabin

Members Present

Table.1 Course committee members

S.No.	Name of the faculty & Designation, Program	Sem/Sec/Program	Signature
1.	Dr.K. Uthradevi ASP/IT - Course coordinator	IV SEM/IT	
2.	Mr. A. Vivek Ignatius	IV SEM// IT	

HOD welcomed all the members present

1. Content of syllabus, unit wise discussed. Nature of qualitative, quantitative, problematic, theoretical concepts etc. have been discussed
2. With reference to the R-2017 regulation, Number of periods per unit = 09, total number of periods = 45 periods. 10 periods allotted for tutorials.
3. Vision and mission of the college, department discussed. POs, PEOs, PSOs discussed.
4. Course outcomes defined for each units, considering learning outcomes.

Table.2 Course Outcomes

CO	Course Outcomes	POs	PSOs
C202.1	Understand the basics structure of computers, operations and instructions.	1,2,3,4,5,6,7,8,9,10,11,12	1,2
C202.2	Design arithmetic and logic unit.	1,2,3,4,5,6,7,8,9,10,11,12	1,2
C202.3	Understand pipelined execution and design control unit.	1,2,3,4,5,6,7,8,9,10,11,12	1,2
C202.4	Understand parallel processing architectures.	1,2,3,4,5,6,7,8,9,10,11,12	1,2
C202.5	Understand the various memory systems and I/O communication	1,2,3,4,5,6,7,8,9,10,11,12	1,2

5. Mapping of COs with POs and PSOs is done with suitable correlation levels(1 for low, 2 for medium, 3 for high,"-" for no correlation, before content beyond syllabus)

Table.3 Mapping of COs, C, PSOs with POs- before CBS.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C202.1	3	2	3	-	2	2	2	-	-	3	-	2	2	2
C202.2	3	-	3	2	-	2	2	-	2	-	-	2	2	2
C202.3	3	-	3	-	-	2	2	-	-	-	2	2	2	2
C202.4	3	2	3	2	2	2	-	-	2	-	-	2	2	2
C202.5	-	-	-	-	-	2	2	-	-	3	2	2	2	2

6. Identification of content beyond syllabus- curricular gaps are identified considering industry needs, employers feedback, alumni feedback, government policy on industrialization, new investments by private/ public sectors, societal needs and level of correlation of COs with POs and PSOs. Accordingly the details of CBS added and its correlation is given below.

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Table.4 Identification of content beyond syllabus

Content beyond syllabus added	POs strengthened/Vacant filled	CO/Unit
Communication Components	PO9 Vaccant Filled	C302.3 & C302.5/III & V

7. Mapping of COs with POs, PSOs- after CBS.

Table.5 Mapping of COs, C, PSOs with POs- after CBS.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C202.1	3	2	3	-	2	2	2	-	-	3	-	2	2	2
C202.2	3	-	3	2	-	2	2	-	2	-	-	2	2	2
C202.3	3	-	3	-	-	2	2	-	2	-	2	2	2	2
C202.4	3	2	3	2	2	2	-	-	2	-	-	2	2	2
C202.5	-	-	-	-	-	2	2	-	2	3	2	2	2	2

8. Content beyond syllabus is thus identified based on the above. Plan for handling of CBS by internal/external resource person/ industrial visits are decided. This will be included in the class log book.
9. Lecture schedule should be prepared unit wise, as in the syllabus. Number of periods per unit and total number of periods planned should not be less than, periods allotted in the syllabus of Anna University.
10. Plan for additional Periods for IA tests, CBS, NPTEL delivery, Seminar, Quiz etc are to be incorporated in the lecture schedule. These periods are added exclusive of number of periods prescribed in the syllabus.
11. Plan for at least three assignments (with level of correlation), seminar topic, quiz questions discussed.
12. Separate tutorial sheets should be prepared and supplied to all students. Minimum two periods per unit to be planned, totally 10 tutorial periods. Minimum 2 tutorial questions should be set per unit, totally 10 tutorial questions.
13. Bright students and slow learners are to be identified, immediately after IA test - 1. such students may be counselled suitably and the evidence for counselling to be recorded in the attendance cum assessment record. (Sign of students with date and time of counselling, to be strictly recorded and to be attached in the course file). Such counselling may be conducted after college hours.
14. For those students secured less than 60% in the IA Test, Makeup test should be conducted. Correspondingly root cause analysis for reasons of failure, corrective and preventive action, and follow up action taken should be filed properly.
15. Contents of course file to be reviewed periodically.
16. Lecture schedule, assignment questions, tutorial questions, course materials, AU questions (at least 5) should be supplied within one week after the commencement of classes.
17. Course material should be uploaded in the college website for student's reference.
18. Discrepancy in question paper, if any to be informed to the controller of examinations through web portal entry, after getting approval from the HoD & the Principal. Critically asked questions, if any to be discussed with the students of the next batch.
19. Immediately after the publication of the results, analysis are to be carried out and follow up action to be taken for the failures.
20. IA test question papers should be set as per the norms of the college, incorporating marks for learning outcomes and course outcomes. Common question papers should be set.
21. Certificate courses/Workshop/guest lectures may be planned inviting experts from industry/higher learning institutions.
22. After IA test, an objective type tests may be conducted (3 times in a semester-30 minutes duration-maximum 10 questions). Questions asked in GATE, TANCET, IES or any other Competitive examination can be taken as a reference. This is to facilitate the bright students to prepare for higher level of thinking and to enhance placement and higher studies opportunities.
23. IA test papers, assignment papers or any other papers submitted by the students, should be returned to the students within 5 days after correction. Sample paper should be suitably filed.
24. Long absentees of students if any to be informed to the parents through class coordinator, if such students attendance less than 75%.

Course coordinator

HoD/IT

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DEPARTMENT OF INFORMATION TECHNOLOGHY

Lecture Schedule

Degree/Program: **B.TECH / IT**
Regution: **2017**

Course code &Name: **CS8491 & CA**
Semester: **IV** Faculty : **Mrs.S. Saroja Devi**

AIM:

To expose the students to principle of operation and performance of electrical machines

OBJECTIVES:

To impart knowledge on

- To learn the basic structure and operations of a computer.
- To learn the arithmetic and logic unit and implementation of fixed-point and floating point arithmetic unit.
- To learn the basics of pipelined execution.
- To understand parallelism and multi-core processors.
- To understand the memory hierarchies, cache memories and virtual memories.
- To learn the different ways of communication with I/O devices..

PREREQUISITES:

Circuit theory, Electromagnetic theory.

COURSE OUTCOMES:

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C402.1	Understand the basics structure of computers, operations and instructions.	1,2,3,4,5,6,7,8,9,10,11,12	1,2
C402.2	Design arithmetic and logic unit.	1,2,3,4,5,6,7,8,9,10,11,12	1,2
C402.3	Understand pipelined execution and design control unit.	1,2,3,4,5,6,7,8,9,10,11,12	1,2
C402.4	Understand parallel processing architectures.	1,2,3,4,5,6,7,8,9,10,11,12	1,2
C402.5	Understand the various memory systems and I/O communication	1,2,3,4,5,6,7,8,9,10,11,12	1,2

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S.No	Date	Topics to be Covered	Book
	UNIT -I BASIC STRUCTURE OF A COMPUTER SYSTEM-	**Target periods :09**	
1	6.2.21	Functional Units	
2	7.2.2	Basic Operational Concepts	
3	7.2.21	Performance	
4	8.2.21	Instructions: Language of the Computer	
5	9.2.21	Operations, Operands	
6	10.2.21	Instruction representation	Online
7	15.2.21	Logical operations	
8	16.2.21	decision making	
9	17.2.21	MIPS Addressing	
10	21.2.21	Tutorial	
11	21.2.21	Tutorial	
UNIT II - ARITHMETIC FOR COMPUTERS		**Target periods :09**	
12	28.2.21	Addition and Subtraction	Online
13	01.3.21	Multiplication	
14	3.3.21	Division	
15	16.3.21	Floating Point Representation	
16	20.3.21	Floating Point Representation	
17	21.3.21	Floating Point Operations	
18	24.3.21	Floating Point Operations	
19	27.3.21	Subword Parallelism	
20	27.3.21	Subword Parallelism	
21	28.3.21	Tutorial	
22	28.3.21	Tutorial	
UNIT III -PROCESSOR AND CONTROL UNIT		**Target Periods :09**	
23	30.3.21	A Basic MIPS implementation	Online
24	31.3.21	Building a Datapath	
25	3.4.21	Control Implementation Scheme	
26	5.4.21	Pipelining	
27	6.4.21	Pipelined datapath and control	
28	10.4.21	Handling Data Hazards & Control Hazards	
39	12.4.21	Handling Data Hazards & Control Hazards	
30	24.4.21	Exceptions.	
31	24.4.21	Tutorial	
32	26.4.21	Tutorial	
UNIT IV - PARALLELISIM		**Target Periods :09**	
33	26.4.21	Parallel processing challenges	Online
34	28.4.21		
35	28.4.21	Flynn's classification	
36	2.5.21	SISD, MIMD, SIMD, SPMD, and Vector Architectures	
37	3.5.21	Hardware multithreading	
38	4.5.21		
39	8.5.21	Multi-core processors and other Shared Memory Multiprocessors	

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40	10.5.21	ntroduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message	
41	10.5.21	Passing Multiprocessors.	
42	12.5.21	Tutorial	
UNIT V - MEMORY & I/O SYSTEMS			**Target Periods:09**
43	12.5.21	Memory Hierarchy	Online
44	15.5.21	memory technologies	
45	15.5.21	cache memory	
46	16.5.21	measuring and improving cache performance	
47	16.5.21	– virtual memory, TLB's	
48	17.5.21	Accessing I/O Devices	
49	17.5.21	Interrupts	
50	18.5.21	Direct Memory Access, Bus structure	
51	18.5.21	Bus operation ,Arbitration , Interface circuits , USB.	
52		Tutorial	
53		Tutorial	
Content Beyond the Syllabus			
54		Communication Component's	Online

Book Reference - Text Books

Sl.	Title of the Book	Author	Publisher	Year
1.	Computer Organization and Design The Hardware/Software Interface,	David A. Patterson and John L. Hennessy,	Fifth Edition, Morgan Kaufmann / Elsevier	2014
2.	Computer Organization and Embedded Systems	. Carl Hamacher, Zvonko Vranesic, Safwat Zaky and Naraig Manjikian,	Sixth Edition, Tata McGraw Hill	2012

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Book

Sl. No	Title of the Book	Author	Publisher	Year
1	Computer Organization and Architecture – Designing for Performance	William Stallings	Pearson Education	2010

Signature of the Faculty in-charge

HoD / IT

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DEPARTMENT OF INFORMATION TECHNOLOGHY

Identification of Curricular Gap & Content Beyond Syllabus(CBS)

Name of the Faculty : Mrs. S. Saroja Devi **Course Code & Name: CS8491 & CA**

Technology Degree & Program: B.TECH /IT **Semester: IV Year: 2020 -2021 /EVEN**

I.Mapping of Course Outcomes with POs & PSOs.(before CBS)

Table.1 Mapping of COs, C, PSOs with POs - before CBS.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C202.1	3	2	3	-	2	2	2	-	-	3	-	2	2	2
C202.2	3	-	3	2	-	2	2	-	2	-	-	2	2	2
C202.3	3	-	3	-	-	2	2	-	-	-	2	2	2	2
C202.4	3	2	3	2	2	2	-	-	2	-	-	2	2	2
C202.5	-	-	-	-	-	2	2	-	-	3	2	2	2	2
C202	3	2	3	2	2	2	2	-	2	3	2	2	2	2

II. Identification of content beyond syllabus.

Table.2 Identification of content beyond syllabus

Details of Content Beyond Syllabus(CBS) added	POs strengthened/ vacant filled	CO/Unit
Communication Components	PO9 (Vacant filled	C202.3 & III

III. Mapping of Course Outcomes with POs & PSOs. (After CBS)

Table.3 Mapping of COs, C, PSOs with POs- after CBS.

Course	PO 1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C202.1	3	2	3	-	2	2	2	-	-	3	-	2	2	2
C202.2	3	-	3	2	-	2	2	-	2	-	-	2	2	2
C202.3	3	-	3	-	-	2	2	-	*2	-	2	2	2	2
C202.4	3	2	3	2	2	2	-	-	2	-	-	2	2	2
C202.5	-	-	-	-	-	2	2	-	*2	3	2	2	2	2
C202	3	2	3	2	2	2	2	-	4	3	2	2	2	2

Signature of the Faculty **HoD/ IT**

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DEPARTMENT OF INFORMATION TECHNOLOGHY

Proof and identification of Content Beyond Syllabus(CBS)

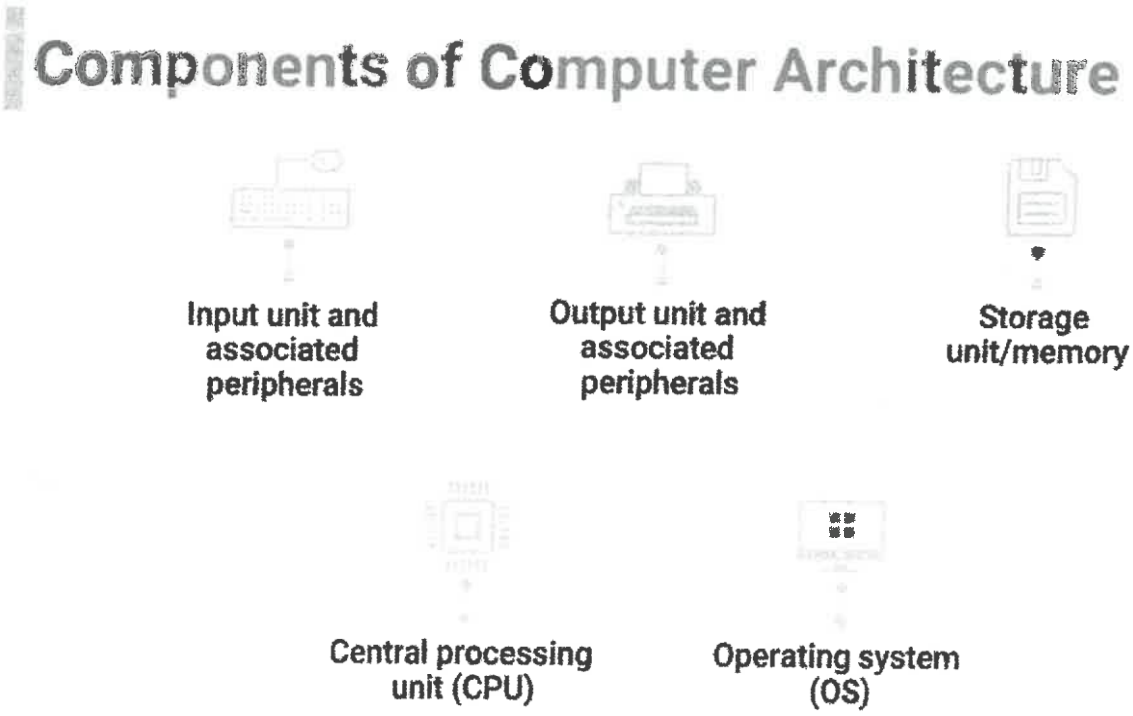
Name of the Faculty : Mrs. S. Saroja Devi
Degree & Program: B.TECH & IT

Course Code & Name: CS8491 & CA
Semester: IV Academic Year: 2020 -2021 /EVEN

TOPIC: Communication Components

Components of Computer Architecture

Depending on the method of categorization, the parts of a computer architecture can be subdivided in several ways. The main components of a computer architecture are the CPU, memory, and peripherals. All these elements are linked by the system bus, which comprises an address bus, a data bus, and a control bus. Within this framework, the computer architecture has eight key components, as described below.



Components of Computer Architecture

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1. Input unit and associated peripherals

The input unit provides external data sources to the computer system. Therefore, it connects the external environment to the computer. It receives information from input devices, translates it to machine language, and then inserts it within the computer system. The keyboard, mouse, or other input devices are the most often utilized and have corresponding hardware drivers that allow them to work in sync with the rest of the computer architecture.

2. Output unit and associated peripherals

The output unit delivers the computer process's results to the user. A majority of the output data comprises music, graphics, or video. Computer architecture's output devices encompass the display, printing unit, speakers, headphones, etc.

To play an MP3 file, for instance, the system reads a number array from the disc and into memory. The computer architecture manipulates these numbers to convert compressed audio data to uncompressed audio data and then outputs the resulting set of numbers (uncompressed audio file) to the audio chips. The chip then makes it user-ready through the output unit and associated peripherals.

Signature of the Faculty

HOD/IT

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DEPARTMENT OF INFORMATION TECHNOLOGHY

Assignment Question Paper

Assignment – 01			Date of Issue:	12.03.2021	Marks	10
Course code	CS8491	Course Title	Computer Architecture			
Year	II	Semester	IV	Date of Submission:	18.03.2021	

Q.No	Questions	CO
1	Subword Parallelism	C202.3
2	Handling Data Hazards & Control Hazards – Exceptions	C202.3

Mark Allocation

Rubrics	Marks Allocated	Marks obtained
Content Quality	6	5
Presentation Quality	2	2
Timely submission	2	2
Total marks	10	9

Name and Signature of the Faculty In-charge

HoD/IT

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
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Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

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DEPARTMENT OF INFORMATION TECHNOLOGHY

Tutorial Question Paper

Tutorial – 01			Date of Issue:	11.04.2021	Marks	10
Course code	CS8491	Course Title	Computer Architecture			
Year	II	Semester	I V	Date of Submission:	26 .04.2021	

Q.No	Questions	CO
1	Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message	C202.4
2	Flynn's classification	C202.4

Name and Signature of the Faculty In-charge

HoD/IT

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NAAC Accredited, 2(F) Status Institution by UGC

Internal Assessment Test - I Even Sem Time Table (Higher Semester) - 2020-21

S.No	Branch	YEAR	22.02.21	23.02.21	24.02.21	25.02.21	26.02.21	27.02.21
1	CIVIL	II						
		III	CE8601 & DSSE	CE8602&SA-II	CE8603&IE	CE8604&HE	EN8592&WWE	
		IV						
2	CSE	II	CS3452&TOC	CS3491&AI	CS3492&DBMS	CS3401&ALG	GE3451&EVS	CS3451&OS
		III	CS8651&IP	CS8691&AI	CS8601&MC	CS8602&CD	CS8603&DS	
		IV	GE8076&PE	CS8080&IRT				
3	EEE	II	EE3404&MPMC	EE3405&EM II	EE3401&TD	EE3403&MI	GE3451&EVS	EE3402&LIC
		III	EE8601&SSD	EE8602&PSG	EE8691&ES	EE8005&SEM	EE8002&DEA	
		IV	EE8015&EEG	EE8018&MCB				
4	ECE	II	EC3452&EMF	EC3401&NS	EC3491&CS	EC3451&LIC	GE3451&EVS	EC3492&DSP
		III	MG8591&POM	EC8651&TLRF	EC8691&MPMC	EC8652&WC	EC8095&VLSI	
		IV	GE8076&PE	EC8094&SATCOM				
5	MECH	II	ME3491&TOM	ME3451 &TE	ME3493 &MT-II	ME3492&H&P	GE3451&EVS	CE3491&SM
		III	ME8651&DTS	ME8691&CAD/CAM	ME8693& HMT	ME8692&FEA	ME8694&HP	
		IV	MG8591&POM	ME8094&CIM				
6	AGRI	II	AI3401&TES	AI3402&SWC	AI3403&SOM	CE3691&HWE	GE3451&EVS	ME3391&TD
		III						
		IV						
7	AI&DS	II	MA3391&PS	AL3452&OS	AL3451&ML	AD3491&FDS	GE3451&EVS	CS3591&CN
		III						
		IV						
8	IT	II	MA8391&PS	CS8491 & CA	GS8192 & DBMS	CS8451&DAA	CS8493 & OS	GE8291& ESE
		III	IT8601&CI	CS8592&OOAD	IT8602&MC	CS8091&BDA	CS8092&CGM	
		IV	GE8076&PE	CS8080&IRT				

Exam cell Coordinator

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

Principal

Register Number:

INDRA GANESAN COLLEGE OF ENGINEERING

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Internal Assessment Exam - I			Date/Session	18.04.2021	Marks	50
Course code	CS8491	Course Title	Computer Architecture			
Regulation	2017	Duration	90 minutes	Academic Year	2020-2021	
Year	II	Semester	IV	Department	IT	

COURSE OUTCOMES

CO1:	To learn the basic structure and operations of a computer
CO2:	To learn the arithmetic and logic unit and implementation of fixed-point and floating point arithmetic unit.
CO3:	To learn the basics of pipelined execution.
CO4:	To understand parallelism and multi-core processors
CO5:	To understand the memory hierarchies, cache memories and virtual memories.
CO6:	To learn the different ways of communication with I/O devices.

Q.No.	Question	CO	BTS
	PART A (Answer all the Questions 10 x 2 = 20 Marks)		
1	What are the components of a computer system?	CO1	K1
2	Give the formula for CPU execution time for a program.	CO1	K2
3	Define Program Counter.	CO1	K2
4	How to represent instruction in a computer system?	CO1	K1
5	State the needs of indirect addressing mode. Give Example.	CO1	K1
6	What do you mean by zero address instruction?	CO1	K1
7	Brief about relative addressing mode with an example.	CO1	K3
8	Subtract$(11010)_2$-$(10000)_2$ using 2's complement method.	CO2	K2
9	Draw the Half-adder circuit.	CO2	K5
10	Write the rule for addition of two binary numbers.	CO2	K2
	PART B (Answer all the Questions 2 x 10 = 20 Marks)		
11a	i. Explain the functional units of a computer in detail. ii. Write note on various types of registers.	CO1	K6
	OR		
11b	Explain the various instruction formats with example.	CO1	K6
12a	Design a full-adder circuit and explain in detail	CO2	K2
	OR		
12b	Explain the Multiplication operation using flowchart and Multiply B=1101 and Q=1011 using the process	CO2	K2
	PART C (Answer all the Questions 1 x 10 = 10 Marks)		
13a	Draw a neat sketch, explain in detail about logic design for carry look-ahead adder	CO1	K2
	OR		
13b	Classify MIPS addressing Modes and give examples for each.	CO1	K2

Course Faculty

(Name /Sign / Date)

HoD

(Name /Sign / Date)

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Internal Assessment Test - I Retest Even Sem Time Table (Higher Semester) 2020 - 21

S.No	Branch	YEAR	1.03.21	2.03.21	3.03.21	4.03.21	5.03.21	6.03.21
1	CIVIL	II						
		III	CE8601 & DSSE	CE8602&SA-II	CE8603&IE	CE8604&HE	EN8592&WWE	
		IV						
2	CSE	II	CS3452&TOC	CS3491&AI	CS3492&DBMS	CS3401&ALG	GE3451&EVS	CS3451&OS
		III	CS8651&IP	CS8691&AI	CS8601&MC	CS8602&CD	CS8603&DS	
		IV	GE8076&PE	CS8080&IRT				
3	EEE	II	EE3404&MPMC	EE3405&EM II	EE3401&TD	EE3403&MI	GE3451&EVS	EE3402&LIC
		III	EE8601&SSD	EE8602&PSG	EE8691&ES	EE8005&SEM	EE8002&DEA	
		IV	EE8015&EEG	EE8018&MCB				
4	ECE	II	EC3452&EMF	EC3401&NS	EC3491&CS	EC3451&LIC	GE3451&EVS	EC3492&DSP
		III	MG8591&POM	EC8651&TLRF	EC8691&MPMC	EC8652&WC	EC8095&VLSI	
		IV	GE8076&PE	EC8094&SATCOM				
5	MECH	II	ME3491&TOM	ME3451 &TE	ME3493 &MT-II	ME3492&II&P	GE3451&EVS	CE3491&SM
		III	ME8651&DTS	ME8691&CAD/CAM	ME8693& HMT	ME8692&FEA	ME8694&HP	
		IV	MG8591&POM	ME8094&CIM				
6	AGRI	II	AI3401&TES	AI3402&SWC	AI3403&SOM	CE3691&HWE	GE3451&EVS	ME3391&TD
		III						
		IV						
7	AI&DS	II	MA3391&PS	AL3452&OS	AL3451&ML	AD3491&FDS	GE3451&EVS	CS3591&CN
		III						
		IV						
8	IT	II	MA8391&PS	CS8491 & CA	CS8492 & DBMS	CS8451&DAA	CS8493 & OS	GE8291& ESE
		III	IT8601&CI	CS8592&OOAD	IT8602&MC	CS8091&BDA	CS8092&CGM	
		IV	GE8076&PE	CS8080&IRT				

Exam cell Coordinator

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Principal

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Internal Assessment Test Answer Book

Name	Tamil Selvi . T			**Year/ Semester/Section**	II / IV
Batch No.	2020 - 2021	**Date/Session**	23.2.21 / FN	**Department**	IT
Course code	CS 8491	**Course Title**	Computer Architecture		
Internal Assessment Test	**IAT 1** ☑	**IAT 2** ☐	**IAT 3** ☐	**Model** ☐	
Name and Signature of the Invigilator with date					

Instruction to the Student: Put tick mark to the question attended in the column against question.

Part A			Part B / Part C					Total Marks
Q. No.	✓	Marks	Q. NO.	✓	a Marks	✓	b Marks	
1	✓	2	11	✓	12			12
2	✓	0	12			✓	10	10
3	✓	1	13			✓	11	11
4	✓	2	14					
5	✓	2	15					
6	✓	2	16					
7	✓	2					Total	33
8	✓	1						
9	✓	1	47					
10	✓	1						
Total		14	Grand Total				Name and Signature of the Examiner with date	

To be filled by the examiner

Course Outcomes	1	2	3	4	5	6	Total
Marks allotted	30	20					50
Marks Obtained	29	18					47

IQAC Audit - Remarks

Name and Signature of the IQAC member

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
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Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

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IQAC Academic Audit Form

ACADEMIC YEAR: 2020-2021 EVEN SEMESTER

Name of Department :	IT	Year / Sem :	III / IV	No. of Students Registered :	20

Details of Examination : IA Test -1 / IA Test -2 / IA Test -3 / Model Test

S.No.	Course Code	List of Reg.No Verified	Course Log Book Verified (Y / N)	Course File Verified (Y / N)	No of students Attended	No of Absentees	No of Failures	Pass %	Remarks
1.	MA8391	811219205003	Y	Y	20	2	0	100%	—
2.	CS8491	811219205019	Y	Y	20	2	1	94%	—
3.	CS8492	811219205012	Y	Y	20	2	0	100%	—
4.	CS8493	811219205501	Y	Y	20	2	2	88%	—
5.	CS8451	811219205506	Y	Y	20	2	0	100%	—
6.	GE8291	811219205517	Y	Y	20	2	0	100%	—

Verified by

External Member Name and Signature: Dr. S. Karthikeyan &

Internal Member Name and Signature: N. KARTHIGA &

Overall Remarks:

HoD/ IT **IQAC Co-ordinator** **Principal**

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
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DEPARTMENT OF INFORMATION TECHNOLOGHY

ROOT CAUSE ANALYSIS

Name of the Faculty : S. Saroja Devi
Degree & Program : B.Tech (IT)
IA Test : I / II / III/ Model

Course code & Name : CS8491 & Computer Architect
Semester & Section : IV Sem
University Exam/
Month & Year : APR/ MAY – 2021

Target : 98%.
Achieved : 90%.

S.NO	ROLL NO	NAME OF THE STUDENT	CAUSES FOR FAILURE	CORRECTIVE ACTION TAKEN	PREVENTIVE ACTION TAKEN	FOLLOWUP STATUS	REMARKS OF THE HOD
1.	811219205016	P. Sowmiya	Stomach Ache	Retest	Special coaching	Yes	–
2.	811219205001	V. Akash	Typhoid	Retest	Special coaching	Yes	–

S. [illegible]
Signature of the Faculty

Signature of the HOD/ IT

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
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Manikandam, Trichy-620 012.