Indra Ganesan
COLLEGE OF ENGINEERING

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai
Accredited by NAAC with 'B+' Grade, 2(f) & 12B Status Institution by UGC
IG Valley, Madurai Main Road, Manikandam, Tiruchirappalli - 620012

NAAC DOCUMENTS

QUALITY INDICATOR FRAME WORK

CRITERION – 1

CURRICULAR ASPECTS

SUBMITTED BY

IQAC

INTERNAL QUALITY ASSURANCE CELL

INDRA GANESAN COLLEGE OF ENGINEERING

Criteria 1	Curricular Aspects	100

1.1 Curricular Planning and Implementation (20)

1.1.1 The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment

Table of Content

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PREFACE OF THE COURSE FILE

Batch	: **2018-2022**
Academic Year	: **2019-2020 / ODD**
Program	: **ELECTRONICS AND COMMUNICATION ENGINEERING**
Year & Semester	: **2nd Year / 3rd Semester**
Course Code	: **EC 8392**
Name of the Course	: **Digital Electronics**
Faculty in-charge	: **Mrs.M.Nandhini, AP/ECE**

Signature of the Faculty in-charge

M. Bhuvaneswari
HoD / ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

EC8392	DIGITAL ELECTRONICS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To present the Digital fundamentals, Boolean algebra and its applications in digitalsystems
- To familiarize with the design of various combinational digital circuits using logic gates
- To introduce the analysis and design procedures for synchronous and asynchronoussequential circuits
- To explain the various semiconductor memories and related technology
- To introduce the electronic circuits involved in the making of logic gates

UNIT I DIGITAL FUNDAMENTALS 9

Number Systems – Decimal, Binary, Octal, Hexadecimal, 1„s and 2„s complements, Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes, Boolean theorems, Logic gates, Universal gates, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map Minimization and Quine-McCluskey method of minimization.

UNIT II COMBINATIONAL CIRCUIT DESIGN 9

Design of Half and Full Adders, Half and Full Subtractors, Binary Parallel Adder – Carry lookahead Adder, BCD Adder, Multiplexer, Demultiplexer, Magnitude Comparator, Decoder, Encoder, Priority Encoder.

UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS 9

Flip flops – SR, JK, T, D, Master/Slave FF – operation and excitation tables, Triggering of FF, Analysis and design of clocked sequential circuits – Design - Moore/Mealy models, state minimization, state assignment, circuit implementation – Design of Counters- Ripple Counters, Ring Counters, Shift registers, Universal Shift Register.

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS 9

Stable and Unstable states, output specifications, cycles and races, state reduction, race freeassignments, Hazards, Essential Hazards, Pulse mode sequential circuits, Design of Hazard free circuits.

UNIT V MEMORY DEVICES AND DIGITAL INTEGRATED CIRCUITS 9

Basic memory structure – ROM -PROM – EPROM – EEPROM –EAPROM, RAM – Static and dynamic RAM - Programmable Logic Devices – Programmable Logic Array (PLA) - Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA) - Implementation of combinational logic circuits using PLA, PAL. Digital integrated circuits: Logic levels, propagation delay, power dissipation, fan-out and fan- in, noise margin, logic families and their characteristics-RTL, TTL, ECL, CMOS

TOTAL: 45 PERIODS

OUTCOMES:

At the end of the course:

- Use digital electronics in the present contemporary world
- Design various combinational digital circuits using logic gates
- Do the analysis and design procedures for synchronous and asynchronous sequentialcircuits
- Use the semiconductor memories and related technology
- Use electronic circuits involved in the design of logic gates

TEXT BOOK:

1. M. Morris Mano and Michael D. Ciletti, "Digital Design", 5th Edition, Pearson, 2014.

REFERENCES:

1. Charles H.Roth. "Fundamentals of Logic Design", 6th Edition, Thomson Learning, 2013.
2. Thomas L. Floyd, "Digital Fundamentals", 10th Edition, Pearson Education Inc, 2011
3. S.Salivahanan and S.Arivazhagan"Digital Electronics", 1st Edition, Vikas Publishing House pvt Ltd, 2012.

4. Anil K.Maini "Digital Electronics", Wiley, 2014.
5. A.Anand Kumar "Fundamentals of Digital Circuits", 4th Edition, PHI Learning PrivateLimited, 2016.
6. Soumitra Kumar Mandal " Digital Electronics", McGraw Hill Education Private Limited, 2016.

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Faculty Time Table

Mrs.M.Nandhini

Day Order	1	2	3	4	5	6	7	8
I								
II			EC8392					
III		EC8392						
IV			EC8392					EC8392
V					EC8392			

S.Code	Title	Year / Branch	Hours
EC8392	Digital Electronics	II/ECE	5
TOTAL - 5 hours			

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Lecture Schedule

Degree/Program: **B.E / ECE**
Duration: **July 2019 – Nov 2019**

Course code &Name: **EC8392**–DIGITAL ELECTRONICS
Semester: **III** Section: **A** Faculty: **Mrs.M,Nandhini**

AIM:

To teach the students about the analysis and design of digital system

OBJECTIVES:

To impart knowledge on

(i) To present the Digital fundamentals, Boolean algebra and its applications in digitalsystems
(ii) To familiarize with the design of various combinational digital circuits using logic gates
(iii) To introduce the analysis and design procedures for synchronous and asynchronoussequential circuits
(iv) To explain the various semiconductor memories and related technology
(v) To introduce the electronic circuits involved in the making of logic gates

PREREQUISITES:

COURSE OUTCOMES:

After the course, the student should be able to:

CO	Course Outcomes	POs	PSOs
C205.1	Use digital electronics in the present contemporary world	1,2,3,4,5,12	3
C205.2	Design various combinational digital circuits using logic gates	1,2,3,4,5,12	2
C205.3	Do the analysis and design procedures for synchronous and asynchronous sequential circuits	1,2,3,4,5,12	1
C205.4	Use the semiconductor memories and related technology	1,2,3,4,5,12	2
C205.5	Use electronic circuits involved in the design of logic gates	1,2,3,4,5,12	3

S.No	Date	Period	Topics to be Covered	Book & Page. No.
UNIT -I - DIGITAL FUNDAMENTALS				Target periods :9
1	02/07/19	3	Number Systems , Decimal, Binary, Octal, Hexadecimal, 1_s and 2_s complements	T1,R3
2	03/07/19	2	Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes	T1
3	04/07/19	3	Boolean theorems, Logic gates, Universal gates	T1 T1,R3
4	05/07/19	5	Problems	T1
5	09/07/19	3	Sum of products and product of sums	T1,R3
6	10/07/19	2	Problems	

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

7	11/07/19	3	Minterms and Maxterms, Karnaugh map	T1
8	11/07/19	8	Minimization and Quine-McCluskey method of minimization	T1
9	12/07/19	5	Problems	T1,R3
UNIT II - COMBINATIONAL CIRCUIT DESIGN				**Target Periods :9**
10	18/07/19	3	Design of Half and Full Adders	T1
11	19/07/19	5	Half and Full Subtractors	T1
12	23/07/19	3	Binary Parallel Adder	T1
13	24/07/19	2	Carry look ahead Adder	T1
14	25/07/19	3	BCD Adder	T1
15	25/07/19	8	Multiplexer, Demultiplexer	T1
16	26/07/19	5	Magnitude Comparator	T1
17	30/07/19	3	Decoder, Encoder, Priority Encoder.	T1, R3
18	31/07/19	2	Problems	**Target Periods :9**
UNIT III - SYNCHRONOUS SEQUENTIAL CIRCUITS				T1
19	06/08/19	3	Flip flops – SR, JK, T, D, Master/Slave FF – operation and excitation tables	T1
20	07/08/19	2	Triggering of FF, Analysis and design of clocked sequential circuits	T1
21	08/08/19	3	Design - Moore/Mealy models, state minimization, state assignment, circuit implementation	T1
22	09/08/19	5	Design - Moore/Mealy models-Contd	T1
23	13/08/19	3	Design of Counters- Ripple Counters	T1, R3
24	14/08/19	2	Problems	T1
25	16/08/19	3	Ring Counters, Shift registers	T1
26	16/08/19	8	Universal Shift Register	T1, R3
27	20/08/19	3	Problems	**Target Periods :9**
UNIT IV - ASYNCHRONOUS SEQUENTIAL CIRCUITS				T1
28	29/08/19	3	Stable and Unstable states	T1
29	30/08/19	5	output specifications, cycles and races, state reduction	T1
30	03/09/19	3	Race free assignments, Hazards, Essential Hazards	T1, R3
31	04/09/19	2	Problems	T1
32	05/09/19	3	Pulse mode sequential circuits	T1, R3
33	06/09/19	5	Problems	T1, R3
34	10/09/19	3	Problems	T1
35	11/09/19	3	Design of Hazard free circuits.	T1, R3
36	11/09/19	8	Problems	**Target Periods:9**
UNIT V - MEMORY DEVICES AND DIGITAL INTEGRATED CIRCUITS				T1
37	17/09/19	3	Basic memory structure , ROM ,PROM , EPROM , EEPROM ,EAPROM, RAM , Static and dynamic RAM	T1
38	18/09/19	2	Programmable Logic Devices – Programmable Logic Array (PLA) - Programmable Array Logic (PAL)	T1
39	19/09/19	3	Field Programmable Gate Arrays (FPGA) - Implementation of combinational logic circuits using PLA, PAL	T1
40	20/09/19	5	Problems	T1
41	25/09/19	2	Digital integrated circuits: Logic levels, propagation delay, power dissipation, fan-out and fan- in, noise margin, logic families and their characteristics-RTL	T1

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

42	25/09/19	8	Logic levels, propagation delay, power dissipation, fan-out and fan- in, noise margin, logic families and their characteristics- TTL	T1
43	25/09/19	3	Logic levels, propagation delay, power dissipation, fan-out and fan- in, noise margin, logic families and their characteristics-ECL	T1
44	26/09/19	8	Logic levels, propagation delay, power dissipation, fan-out and fan- in, noise margin, logic families and their characteristics-CMO	T1
45	27/09/19	5	Problems	T1, R3
			Content Beyond the Syllabus	
46	01/10/19	3	Advanced Field Programmable Gate Array	Material

Book Reference - Text Books

Sl.	Title of the Book	Author	Publisher	Year
1.	Digital Design	M. Morris Mano and Michael D. Ciletti	5th Edition ,Pearson	2014

Book Reference- References

Sl	Title of the Book	Author	Publisher	Year
1.	Fundamentals of Logic Design	Charles H.Roth	6th Edition, Thomson Learning	2013
2.	Digital Fundamentals	Thomas L. Floyd	10th Edition, Pearson Education	2011
3.	Digital Electronics	S.Salivahanan and S.Arivazhagan	Ist Edition, Vikas Publishing House pvt Ltd,	2012

Website References:

1.https://onlinecours in/noc22_ee55

Signature of the Faculty in-charge

M. Bhuvaneswari
HoD / ECE

Dr. G. Balakrishnan, M.E., Ph.D.
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Identification of Curricular Gap & Content Beyond Syllabus(CBS)

Name of the Faculty :Mrs.M.Nandhini **Course Code & Name:EC8392-Digital Electronics**

Degree & Program:B.E. /ECE **Semester & Section: III / A** **Academic Year: 2019 -2020 /ODD**

I.Mapping of Course Outcomes with POs & PSOs.(before CBS)

Table.1 Mapping of COs, C, PSOs with POs - before CBS.

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C205.1	3	3	3	2	-	2	-	-	-	-	2	3	2	3	2
C205.2	3	3	3	2	-	2	-	-	-	-	2	1	2	3	2
C205.3	3	3	3	2	-	2	-	-	-	-	2	2	2	3	2
C205.4	3	3	3	2	-	2	-	-	-	-	2	2	2	3	2
C205.5	3	3	3	2	-	2	-	-	-	-	2	2	2	3	2
C205.6	3	3	3	2	-	2	-	-	-	-	2	2	2	3	2
C205	3	3	3	2	-	2	-	-	-	-	2	2	2	3	2

II. Identification of content beyond syllabus.

Table.2 Identification of content beyond syllabus

Details of Content Beyond Syllabus(CBS) added	POs strengthened/ vacant filled	CO/Unit
Advanced Field Programmable Gate Array	PO5 vacant filled	C205.6/V

III. Mapping of Course Outcomes with POs & PSOs. (After CBS)

Table.3 Mapping of COs, C, PSOs with POs- after CBS.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C203.1	3	3	3	2	-	2	-	-	-	-	2	3	2	3	2
C203.2	3	3	3	2	-	2	-	-	-	-	2	1	2	3	2
C203.3	3	3	3	2	-	2	-	-	-	-	2	2	2	3	2
C203.4	3	3	3	2	-	2	-	-	-	-	2	2	2	3	2
C203.5	3	3	3	2	*2	2	-	-	-	-	2	2	2	3	2
C203.6	3	3	3	2	-	2	-	-	-	-	2	2	2	3	2
C203	3	3	3	2	-	2	-	-	-	-	2	2	2	3	2

Signature of the Faculty

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

HoD/ECE

INDRA GANESAN COLLEGE OF ENGINEERING

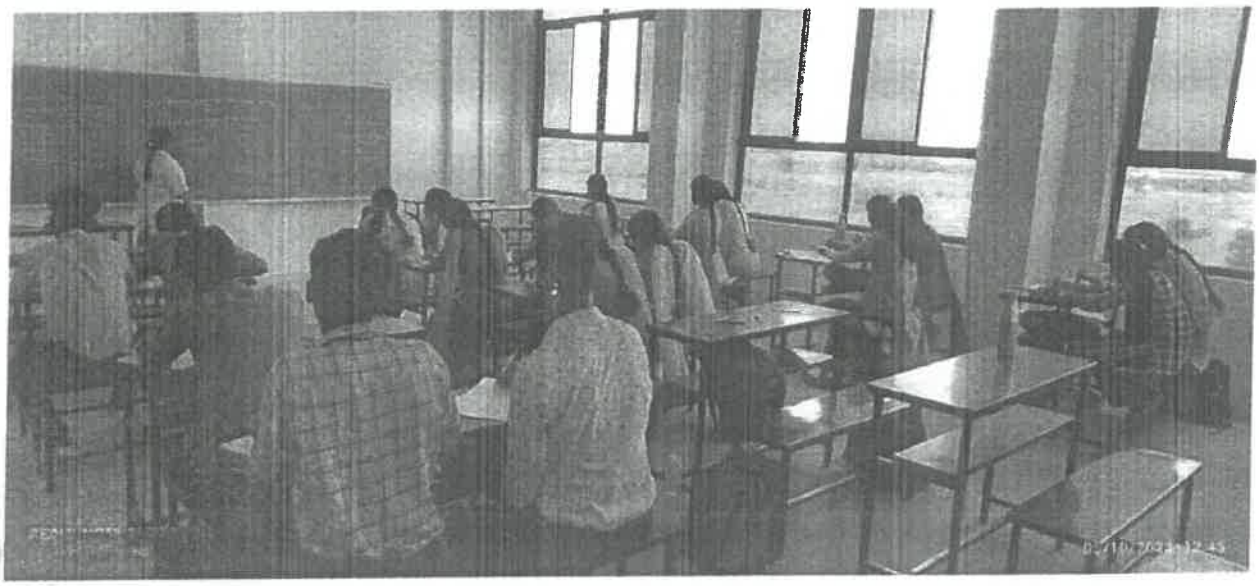
IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

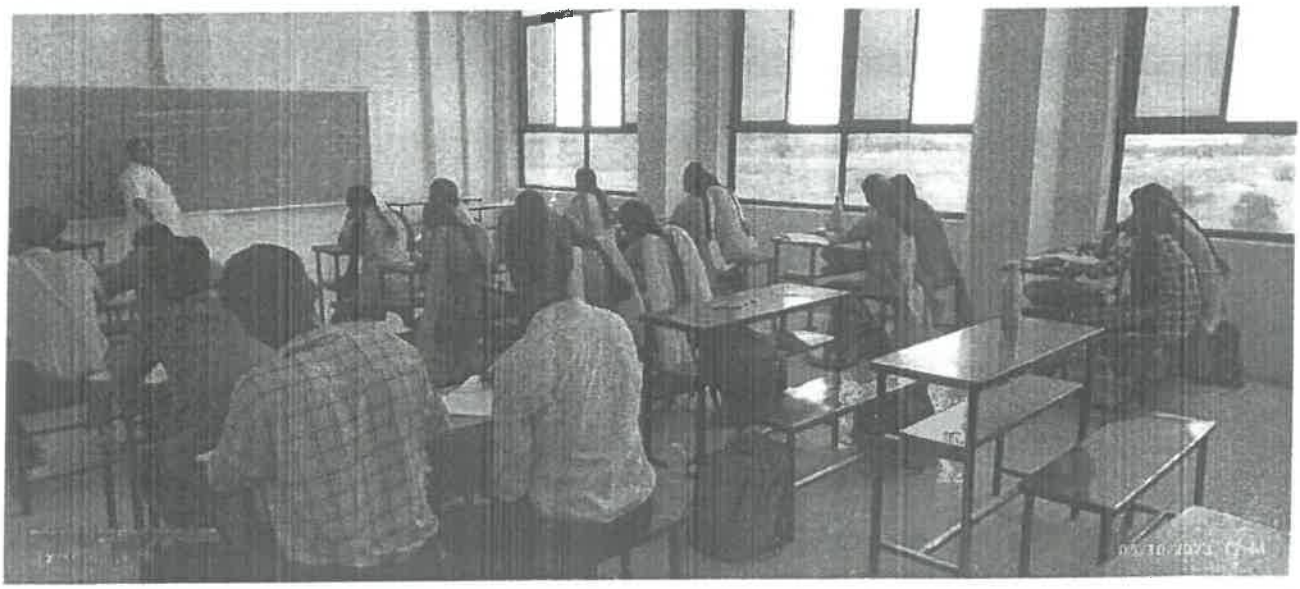
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Proof of Curricular Gap & Content Beyond Syllabus(CBS)

Name of the Faculty :Mrs.M.Nandhini **Course Code & Name:EC8392- Digital Electronics**

Degree & Program:B.E. /ECE **Semester & Section: III / A** **Academic Year: 2019 -2020/ODD**





Signature of the Faculty

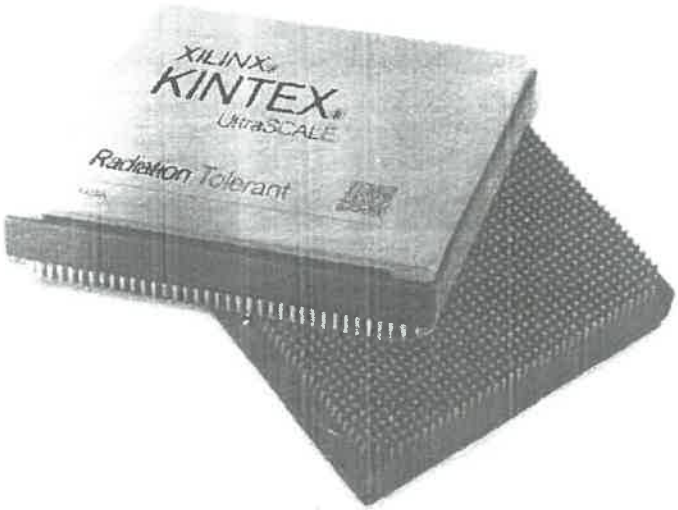
Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

M. Bhuvaneswari
HoD/ECE

Field Programmable Gate Array

What is an FPGA?

FPGA is a term formed by combining the first letters of the word Field-Programmable Gate Array. The reason for using the term "field programming" is that the function of the FPGA integrated circuit (IC) is not programmed at factory output and is an IC that can be changed while in the field. The function mentioned here is a task created with the hardware architecture of IC. It has grown very rapidly since the FPGA term was introduced. While growing at a high rate in terms of capacity and performance, the decrease in cost per unit operation has made FPGAs remarkable (Unlersen, 2015). In Figure 1, an FPGA IC is presented.



An FPGA IC belongs Xilinx Company

Although Xilinx presented the first hardware that can be called FPGA in 1984, the term FPGA became popular in 1988 with the company Actel. The non-recurring engineering cost required for application-specific integrated circuit (ASIC) fabrication does not exist in FPGAs. But, this situation made FPGAs advantageous only in the use of a low number of units. In this process, ASICs were more popular because they were very low cost compared to FPGAs in high production. However, according to Moore's law, the prediction that the number of units that FPGA will be advantageous will increase in the future has prevented the interest in FPGAs from decreasing. Today, performance, I/O capacity, power consumption, time to market and other capabilities are more important than device cost in FPGA-ASIC comparison (*FPGA Designs with VHDL Documentation,*

n.d.; Trimberger, 2015; *What Is an FPGA? Field Programmable Gate Array*, n.d.).

Some of the application areas of FPGAs can be listed as follows (Rajewski, 2017):

- Aerospace
- Defense
- Automotive
- High Performance Computing and Data Storage
- Data Center
- Industrial
- ASIC Prototyping
- Broadcast
- Video and Image Processing
- Wired and Wireless Communications
- Medical Imaging
- Security

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

In the design of an embedded system, the question of which platform should be designed first comes to mind. Because for the designer, there are many different hardware such as microcontrollers, ASIC, microcomputer, FPGA. Actually, FPGA is not a one-to-one alternative to other microprocessor-built platforms. On an FPGA, a hardware to perform the required operation can be designed. However, in systems created with a microprocessor, commands that will perform a desired operation are executed on a fixed hardware. Additionally, it is also possible to design a microprocessor with an FPGA.

The designer's choice of FPGA among these alternatives depends on the needs of the system to be designed rather than a matter of whim. For example, in a hardware where the algorithm to be used will change frequently and operations such as multiplication and division with complex numbers will be made frequently, using a DSP produced for this purpose may be more logical than using an FPGA. Because it will be very simple and flexible to make calculations on this DSP using a high-level language such as C. In a platform that should be cheap rather than high performance, choosing a microcontroller can be a fast, simple and satisfying solution. However, if the process requires high performance and speed, then FPGA will be more suitable for this type of applications

FPGA Structure

FPGAs are semi-ready silicon devices that can be electrically programmed to be part of a digital circuit or system. Its structure can be defined in three main parts: programmable logic blocks, input and output blocks surrounding this block array, and interconnections (Chu, 2008; Gunes & Ors, n.d.).

The basic FPGA structure consists of thousands of basic elements called Configurable Logic Blocks (CLB). These basic structures can be called Logic Blocks (LB), Logic Elements (LE) or Logic Cells (LC) according to the manufacturer (Gunes & Ors, n.d.). CLBs are formed by combining a set of logic elements such as a LookUp Table (LUT) and flip flops (FF). The hardware architecture of the FPGA consists of the data stored in these LUTs. The working principle of a 4-input LUT is illustrated in Figure 2.

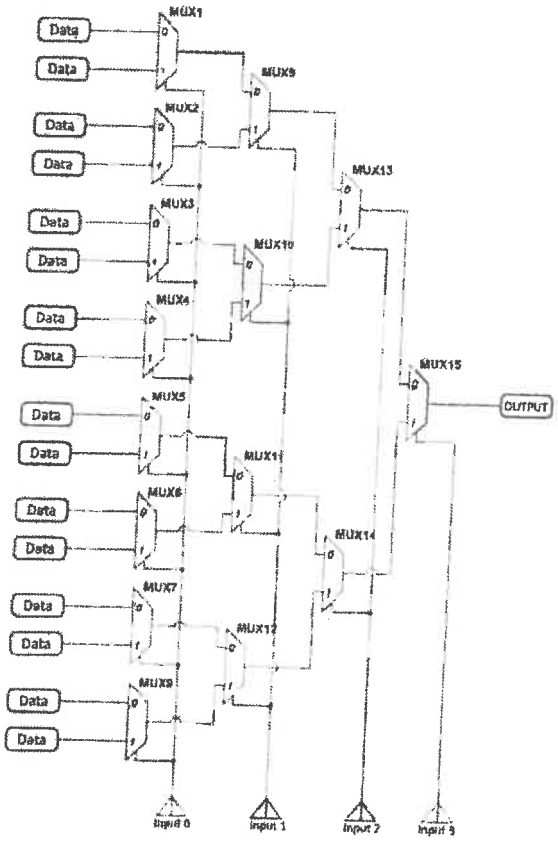


Figure 2. A 4-Input LUT Structure

The values specified here, as Data are the data loaded during FPGA programming. According to this loaded data, the value applied to the inputs is selected and transferred to the output. Thus, this LUT fulfills its special mission.

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Assignment Question Paper

Assignment – 01			Date of Issue:	12.07.2019	Marks	10
Course code	EC8392	Course Title	Digital Electronics			
Year	II	Semester/Section	III/ A	Date of Submission:	19.07.2019	

Q.No	Questions	CO
1	Reduce A(A+B)	C205.1
2	Prove that ABC+ABC'+AB'C+A'BC=AB+AC+BC	C205.1
3	Simplify the following switching function using karnaugh map, $F(A,B,C,D) = \sum (0,5,7,8,9,10,11,14,15) + \Phi (1,4,13)$	C205.1
4	Simplify the Boolean function using K-map and tabular methods. Compare the methods. $F(A, B, C, D) = \sum m(4,5,6,7,8)\ d(A, B, C, D) = \sum m(11,12,13,14,15)$.	C205.1

M. Nandhini & Team

Name and Signature of the Faculty Incharge

H. Bhuvaneswari

HoD/ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Assignment Answer Sheet

Name of the Student : Akila K

AU Register Number: 811218106002

Assignment – 01			Date of Issue:	10.07.2019	Marks	10
Course code	EC8392	Course Title	Digital Electronics			
Year	II	Semester/Section	III/ A	Date of Submission:	15.07.2019	

Q.No	Questions	CO
1	Reduce A(A+B)	C205.1
2	Prove that ABC+ABC'+AB'C+A'BC=AB+AC+BC	C205.1
3	Simplify the following switching function using karnaugh map, $F(A,B,C,D) = \sum (0,5,7,8,9,10,11,14,15) + \Phi (1,4,13)$	C205.1
4	Simplify the Boolean function using K-map and tabular methods. Compare the methods. $F(A, B, C, D) = \sum m(4,5,6,7,8)$ d $(A, B, C, D) = \sum m(11,12,13,14,15)$.	C205.1

Mark Allocation

Rubrics	Marks Allocated	Marks obtained
Content Quality	6	5
Presentation Quality	2	1
Timely submission	2	2
Total marks	10	8

M. Nandhini & Imaad
Name and Signature of the Faculty Incharge

M. Bhuvaneswari
HoD/ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

Register Number:											

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India

(Approved by AICTE, New Delhi and affiliated to Anna University, Chennai)

Internal Assessment Exam - II			Date/Session	03.08.2019/FN	Marks	50
Course code	EC8392	Course Title	Digital Electronics			
Regulation	2017	Duration	90 minutes	Academic Year	2019-2020	
Year	II	Semester	III	Department	ECE	

COURSE OUTCOMES

CO1:	Use digital electronics in the present contemporary world
CO2:	Design various combinational digital circuits using logic gates
CO3:	Do the analysis and design procedures for synchronous and asynchronous sequential circuits
CO4:	Use the semiconductor memories and related technology
CO5:	Use electronic circuits involved in the design of logic gates
CO6:	Design and analyze Logic gates with different technologies

Q.No.	Question	CO	BTS
	PART A **(Answer all the Questions 10 x 2 = 20 Marks)**		
1	Suggest a solution to overcome the limitation on the speed of an adder.	CO2	K1
2	Write an expression for borrow and difference in a full subtractor circuit.	CO2	K1
3	Design a single bit magnitude comparator to compare two words A and B	CO2	K2
4	What is an encoder?	CO2	K1
5	List few applications of multiplexer.	CO2	K1
6	Design a half subtractor using basic gates.	CO2	K2
7	Draw the logic diagram of a 4 line to 1 line multiplexer	CO2	K2
8	What is priority Encoder?	CO2	K1
9	Write down the difference between demultiplexer and decoder.	CO2	K1
10	Give examples for combinational circuit.	CO2	K1
	PART B 2 **(Answer all the Questions 2 x 10 = 20 Marks)**		
11a	Design a 2-bit magnitude comparator and explain its operation in detail	CO2	K2
	OR		
11b	Design a carry look ahead adder with necessary diagrams	CO2	K2
12a	Draw the diagram and explain 1 to 16 Demultiplexer circuit	CO2	K2
	OR		
12b	Implement the function F(A,B,C,D)= $\sum$m(0,1,4,7,6,9) using a 8:1 Multiplexer	CO2	K2
	PART C **(Answer all the Questions 1 x 10 = 10 Marks)**		
13a	Explain how a full adder can be built using two half adders?	CO2	K2
	OR		
13b	Design 7 Segment Display Decoder Circuit?	CO2	K2

Course Faculty

(Name /Sign / Date)

(M. NANDHINI)

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

HoD

(Name /Sign / Date)

Register Number:

INDRA GANESAN COLLEGE OF ENGINEERING

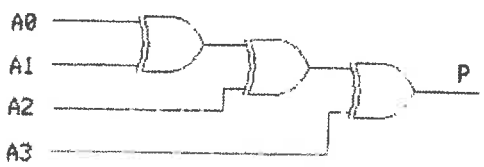
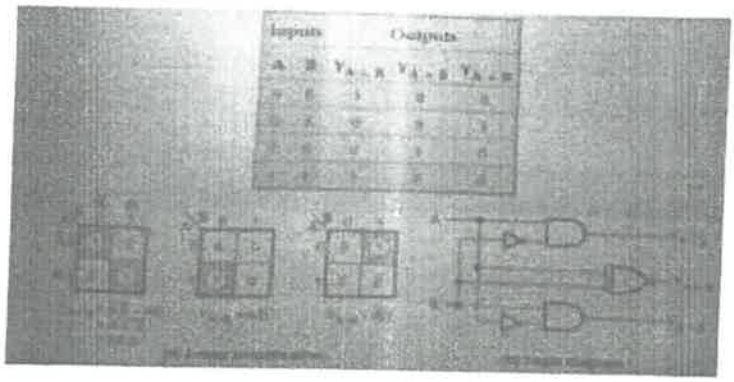
IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India

(Approved by AICTE, New Delhi and affiliated to Anna University, Chennai)

Internal Assessment Exam - II -Key Note			Date/Session	03.08.2019/AN	Marks	50
Course code	EC8392	Course Title	Digital Electronics			
Regulation	2017	Duration	90 minutes	Academic Year	2019-2020	
Year	II	Semester	III	Department	ECE	

COURSE OUTCOMES

CO1:	Use digital electronics in the present contemporary world
CO2:	Design various combinational digital circuits using logic gates
CO3:	Do the analysis and design procedures for synchronous and asynchronous sequential circuits
CO4:	Use the semiconductor memories and related technology
CO5:	Use electronic circuits involved in the design of logic gates
CO6:	Design and analyze Logic gates with different technologies

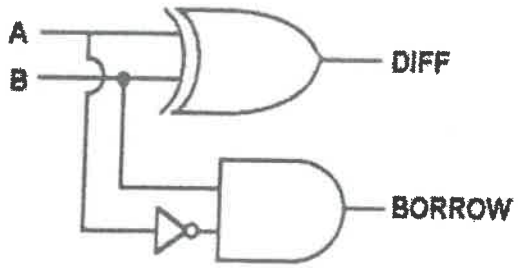
Q.No.	Question	CO	BTS
	PART A (Answer all the Questions 10 x 2 = 20 Marks)		
1	Suggest a solution to overcome the limitation on the speed of an adder. It is possible to increase speed of adder by eliminating inter-stage carry delay. This method utilizes logic gates to look at the lower-order bits of the augend and addend tosee if a higher-order carry is to be generated.	CO2	K1
2	**Write an expression for borrow and difference in a full subtractor circuit.** Difference = $A'B+AB'=A\oplus B$ Borrow = $A'B$	CO2	K1
3	**Design a single bit magnitude comparator to compare two words A and B.**  	CO2	K2
4	**What is an encoder?** An encoder has 2^n input lines and n output lines. In encoder the output lines generatethe binary code corresponding to the input value.	CO1	K1
5		CO2	K1

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

List few applications of multiplexer.

- Data Selector.
- Implement combinational logic circuit.
- Time multiplexing systems
- Frequency multiplexing systems.
- D/A and A/D converter
- Data acquisition systems.

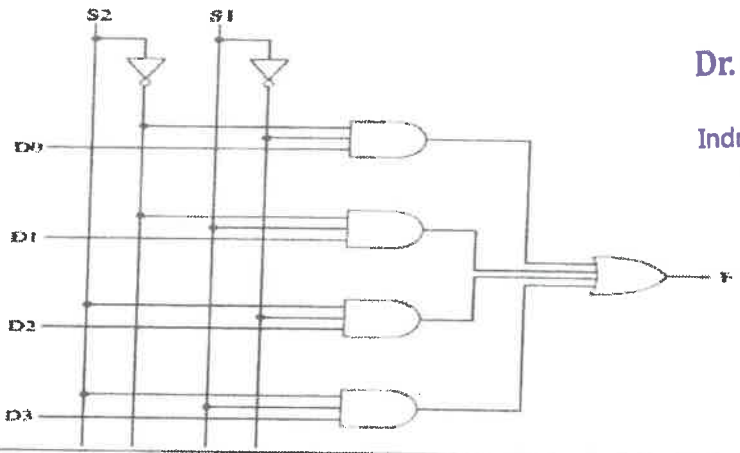
6 Design a half subtractor using basic gates. CO2 K2



Difference=A′B +AB′=A⊕B

Borrow=A′B

7 Draw the logic diagram of a 4 line to 1 line multiplexer. CO2 K2



Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

8 **What is priority Encoder?** CO2 K1

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

9 **Write down the difference between demultiplexer and decoder.** CO2 K1

	Demultiplexer	Decoder
Definition	1 data input2^n outputs	It has n inputs2^n outputs It has n control inputs
Characteristic	Connects the data input tothe data output	Selects one of the 2^n outputs by decoding the binary value on the basis ofn inputs
Reverse of	Multiplexer	Encoder

10	Give examples for combinational circuit. i. Adders ii. Subtractors iii. Multiplexers iv. Demultiplexers v. Encoders vi. Decoders	CO2	K1
	PART B 2 **(Answer all the Questions 2 x 10 = 20 Marks)**		
11a	Design a 2-bit magnitude comparator and explain its operation in detail	CO2	K2
	OR		
11b	Design a carry look ahead adder with necessary diagrams	CO2	K2
12a	Draw the diagram and explain 1 to 16 Demultiplexer circuit	CO2	K2
	OR		
12b	Implement the function F(A,B,C,D)= ∑m(0,1,4,7,6,9) using a 8:1 Multiplexer	CO2	K2
	PART C **(Answer all the Questions 1 x 10 = 10 Marks)**		
13a	Explain how a full adder can be built using two half adders?	CO2	K2
	OR		
13b	Design 7 Segment Display Decoder Circuit?	CO2	K2

Course Faculty

(Name /Sign / Date)

CH. NANDHINI

HoD

(Name /Sign / Date)

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

IG VALLEY, MANIDANDAM, TIRUCHIRAPPALLI – 620 012

ARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2019 – 2020 (ODD SEMESTER)

STUDENTS MARK STATEMENT- CO BASED

CYCLE TEST II

SUBJECT CODE &TITLE: EC8392 & Digital Electronics

YEAR/SEM: II/III

MONTH & YEAR: JULY & 2019

S.NO	REG NO	STUDENT NAME	CO2	Retest CO2	TOTAL (50)	TOTAL (100)
1.	811218106001	Abinaya R	39		39	78
2.	811218106002	Akila K	39		39	78
3.	811218106003	Annie Shalom S	31		31	62
4.	811218106004	Arthi M	39		39	78
5.	811218106005	Azhagu Meena M	35		35	70
6.	811218106006	Devi K	15	30	15	30
7.	811218106007	Dhanalakshmi S	35		35	70
8.	811218106008	Hari Krishnan S	17	32	17	34
9.	811218106009	Janani V	31		31	62
10.	811218106010	Jenifer C	33		33	66
11.	811218106011	Jenifer S	30		30	60
12.	811218106012	Kesavamurthi M	31		31	62
13.	811218106013	Kiruthika S	39		39	78
14.	811218106015	Maria Francis D	38		38	76
15.	811218106016	Ragavi A	41		41	82
16.	811218106017	Ruthramoorthy M	32		32	64
17.	811218106018	Sabarinathan K	31		31	62

Dr. G. Balakrishnan, M...
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

18.	811218106019	Sarmila M	41		41	82
19.	811218106020	Sumathi S	20	31	20	40
20.	811218106021	Thivya Priya R	30		30	60

MARKS RANGE:

<20	20-30	31-40	41-50	51-60	61-70	71-80	81-90	91-100
	1	2		2	8	5	2	

Total No.of Candidates Present	**20**
Total No.of Candidates Absent	**NIL**
Total No.of Students Pass	**17**
Total No. of Students Fail	**03**
Percentage of Pass	**85**

STAFF INCHARGE

HoD/ECE

PRINCIPAL

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 622 012, India

(Approved by AICTE, New Delhi and affiliated to Anna University, Chennai)

Internal Assessment Test Answer Book

Name	M. Sasmila			**Year/ Semester/Section**	II/III/A
Batch No. Reg no.	811218106049	**Date/Session**	03/08/19/AN	**Department**	ECE
Course code	EC8392	**Course Title**	Digital Electronics		
Internal Assessment Test	**IAT 1** ☐	**IAT 2** ☑	**IAT 3** ☐	**Model** ☐	
Name and Signature of the Invigilator with date	K. Kumar 3/8/19 K. KUMAR				

Instruction to the Student: Put tick mark to the question attended in the column against question.

Part A			Part B / Part C					Total Marks
Q. No.	✓	Marks	Q. NO.	✓	a Marks	✓	b Marks	
1	✓	2	11		4		4	8
2	✓	2	12		9			9
3	✓	2	13		8			8
4	✓	2	14					
5	✓	2	15					
6	✓	1½	16					
7	✓	2					Total	24
8	✓	1½						
9	✓	2						
10		—						
Total		17	Grand Total		41/50		Name and Signature of the Examiner with date	5/8/19 (M. NANDHINI)

To be filled by the examiner							
Course Outcomes	1	2	3	4	5	6	Total
Marks allotted		50					
Marks Obtained		41					

IQAC Audit - Remarks

Good. Try to get high marks

Name and Signature of the IQAC member

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India

(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ROOT CAUSE ANALYSIS

Name of the Faculty : M. Nandhini
Degree & Program : B.E & ECE
IA Test : I (II)III/Model
Target : 85%

Course Code & Name : EC8392 & Digital Electronics
Semester & Section : III & A
University Exam/Month & Year: NOV/Dec 2019
Achieved : 70%

S.NO	BATCH NO Reg. No.	NAME OF THE STUDENT	CAUSES FOR FAILURE	SIGNATURE OF THE STUDENT WITH DATE	CORRECTIVE ACTION TAKEN	PREVENTIVE ACTION TAKEN	FOLLOWUP STATUS	REMARKS OF THE HOD
1.	811218106006	Devi. K	Health issue	Devi 10/08/19	Retest conducted	advised to take care of her health	Progress monitored	—
2.	811218106008	Harikrishnan S	Grand mothers health issue	Harikrish 10/08/19	Retest conducted	Advised to take care of grandmothers health	Progress monitored	—
3.	811218106020	Sumathi S	Health issue	Sumathi 10/08/19	Retest conducted	Advised to take care	Progress monitored	—

Signature of the Faculty Member

Dr. G. Balakrishnan, M.E., Ph.D.
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

M. Bhuvaneswari
Signature of the HoD/ECE

INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India
(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

IQAC Academic Audit Form

ACADEMIC YEAR: 2019 – 2020 / EVEN SEMESTER

Name of Department :	ECE	Year / Sem / Sec :	IV / / A	No. of Students Registered :	

Details of Examination : IA Test -1 / IA Test -2 / IA Test -3 / Model Test

S.No.	Course Code	List of Reg.No Verified	Course Log Book Verified (Y / N)	Course File Verified (Y / N)	No of students Attended	No of Absentees	No of Failures	Pass %	Remarks
1	MA8352	811218106016	Y	Y	18	02	3		Retest
2	EC8393	811218106004	Y	Y	20	-	-		-
3	EC8351	811218106016	Y	Y	18	2	1		Retest
4	EC8352	811218106019	Y	Y	20	-	2	90	-
5	EC8392	811218106019	Y	Y	20	-	3	85%	Retest
6	EC8391	811218106016	Y	Y	20	-	2	90	Retest

Verified by

External Member Name and Signature:	K. Seetharaman & K. Seetharaman
Internal Member Name and Signature:	K. Kumar, K. Kumar

Overall Remarks:

M. Bhuvaneswari
HoD/ ECE

IQAC Co-ordinator

Principal

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.