# Indra Ganesan
## COLLEGE OF ENGINEERING

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai
Accredited by NAAC with 'B+' Grade, 2(f) & 12B Status Institution by UGC
IG Valley, Madurai Main Road, Manikandam, Tiruchirappalli - 620012

# NAAC DOCUMENTS

## QUALITY INDICATOR FRAME WORK

## CRITERION – 1

## CURRICULAR ASPECTS

SUBMITTED BY

IQAC

INTERNAL QUALITY ASSURANCE CELL

INDRA GANESAN COLLEGE OF ENGINEERING

| Criteria 1 | Curricular Aspects | 100 |
|---|---|---|

## 1.1 Curricular Planning and Implementation (20)

### 1.1.1 The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment

**Table of Content**


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|---|---|
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# INDRA GANESAN COLLEGE OF ENGINEERING

**IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India**
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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## PREFACE OF THE COURSE FILE

Batch : 2016-2020

Academic Year : 2018-2019 / EVEN

Program : ELECTRONICS AND COMMUNICATION ENGINEERING

Year & Semester : 3rd Year / 6th Semester / 'B' Section

Course Code : EC 6601 NBA Course Code: C312

Name of the Course : VLSI DESIGN

Faculty in-charge : Ms.M.NANDHINI/ AP / ECE

M. Nandhini
Signature of the Faculty in-charge

N. Balajothi
HoD / ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## Syllabus

**EC6601 VLSI DESIGN** **L T P C 3 0 0 3**

**OBJECTIVES:**

In this course, the MOS circuit realization of the various building blocks that is common to any
• microprocessor or digital VLSI circuit is studied. Architectural choices and performance tradeoffs involved in designing and realizing the circuits
• in CMOS technology are discussed. The main focus in this course is on the transistor circuit level design and realization for digital
• operation and the issues involved as well as the topics covered are quite distinct from those encountered in courses on CMOS Analog IC design.

**UNIT I MOS TRANSISTOR PRINCIPLE** 9

NMOS and PMOS transistors, Process parameters for MOS and CMOS, Electrical properties of CMOS circuits and device modeling, Scaling principles and fundamental limits, CMOS inverter scaling, propagation delays, Stick diagram, Layout diagrams

**UNIT II COMBINATIONAL LOGIC CIRCUITS** 9

Examples of Combinational Logic Design, Elmore"s constant, Pass transistor Logic, Transmission gates, static and dynamic CMOS design, Power dissipation – Low power design principles

**UNIT III SEQUENTIAL LOGIC CIRCUITS** 9

Static and Dynamic Latches and Registers, Timing issues, pipelines, clock strategies, Memory architecture and memory control circuits, Low power memory circuits, Synchronous and Asynchronous design

**UNIT IV DESIGNING ARITHMETIC BUILDING BLOCKS** 9

Data path circuits, Architectures for ripple carry adders, carry look ahead adders, High speed adders, accumulators, Multipliers, dividers, Barrel shifters, speed and area tradeoff

**UNIT V IMPLEMENTATION STRATEGIES** 9

Full custom and Semi custom design, Standard cell design and cell libraries, FPGA building block architectures, FPGA interconnect routing procedures.

TOTAL: 45 PERIODS

**OUTCOMES:**

Upon completion of the course,
students should Explain the basic CMOS circuits and the CMOS process technology.
• Discuss the techniques of chip design using programmable devices.

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

- Model the digital system using Hardware Description Language.

**TEXTBOOKS:**

1. Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.
2. M.J. Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997

**REFERENCES:**

1. N.Weste, K.Eshraghian, "Principles of CMOS VLSI Design", Second Edition, Addision Wesley 1993
2. R.Jacob Baker, Harry W.LI., David E.Boyee, "CMOS Circuit Design, Layout and Simulation", Prentice Hall of India 2005
3. A.Pucknell, Kamran Eshraghian, "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007.

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## Faculty Time Table

| Ms.M.Nandhini | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Day Order** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** |
| **I** | | **EC6601** | | | | | | |
| **II** | **EC6601** | | | | | | | |
| **III** | | | | | | | | |
| **IV** | | | EC6601 | | | | | |
| **V** | | **EC6601** | | | | | | |

| **S.Code** | **Title** | **Year / Branch** | **Hours** |
|---|---|---|---|
| EC6601 | VLSI DESIGN | III / ECE B | 4 |
| | | | |
| TOTAL - 4 hours | | | |

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**Lecture Schedule**

Degree/Program: **B.E / ECE**
Duration: **Dec 2018 - Apr 2019**

Course code &Name: **EC6601** –VLSI Design
Semester: **VI** Section: **B** Faculty : **Ms.M.Nandhini**

**AIM:**

To expose the students to principle of operation and performance of VLSI circuits and design

**OBJECTIVES:**

- Understand the fundamentals of IC technology components and their characteristics
- Understand combinational logic circuits and design principles.
- Understand sequential logic circuits and clocking strategies
- Understand Memory Architecture and building blocks
- Understand ASIC Design functioning and design

**PREREQUISITES:** Electronic Devices, Digital Electronics

**COURSE OUTCOMES:**

After the course, the student should be able to:

| CO | Course Outcomes | POs | PSOs |
|---|---|---|---|
| C302.1 | In depth knowledge of MOS technology | 1,2,3,4,11,12 | 1,2,3 |
| C302.2 | Explain the Combinational Logic Circuits and Design Principles | 1,2,3,4,11,12 | 1,2,3 |
| C302.3 | Explain Sequential Logic Circuits and Clocking Strategies | 1,2,3,4,11,12 | 1,2,3 |
| C302.4 | Explain the Memory architecture and building blocks | 1,2,3,4,11,12 | 1,2,3 |
| C302.5 | Apply the ASIC Design Process and Testing | 1,2,3,4,11,12 | 1,2,3 |
| C302.6 | Design using Programmable Devices (ROM, PLA, FPGA), | 1,2,3,4,11,12 | 1,2,3 |

| S.No | Date | Period | Topics to be Covered | Book & Page. No. |
|---|---|---|---|---|
| UNIT -I - Introduction to MOS Transistor Principle | | | Target periods :09 | |
| 1 | 17.12.18 | 2 | Process parameters for MOS and CMOS | 1(12-16) |
| 2 | 18.12.18 | 1 | Electrical properties of CMOS circuits | 1(17-20) |
| 3 | 20.12.18 | 3 | Device Modeling | 1(30-34) |
| 4 | 21.12.18 | 2 | Scaling principles and fundamental limits | |
| 5 | 22.12.18 | 1 | CMOS inverter,scaling | 1(25-27) |
| 6 | 24.12.18 | 2 | Propagation Delays | 1(31-32) |
| 7 | 27.12.18 | 3 | Stick diagram | 1(33-35) |
| 8 | 28.12.18 | 2 | Stick diagram-Contd | 1(35-36) |

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

| | | | | |
|---|---|---|---|---|
| 9 | 29.12.18 | 1 | Layout diagrams | 1(38-39) |
| UNIT II - Introduction to Combinational Logic Circuits | | | Target periods :09 | |
| 10 | 04.01.19 | 2 | Examples of Combinational Logic Design | 1(54-62)<br>2(2-4) |
| 11 | 05.01.19 | 1 | Elmore"s constant | 1(62-71)<br>2(20-28) |
| 12 | 07.01.19 | 2 | Pass transistor Logic | 1(71-91) |
| 13 | 08.01.19 | 1 | Transmission gates | 2(29-34,66-70) |
| 14 | 10.01.19 | 3 | Examples | 1(101-106) |
| 15 | 11.01.19 | 2 | Static and Dynamic CMOS Design | 1(124-125) |
| 16 | 18.01.19 | 2 | Power dissipation | 1(116-120) |
| 17 | 19.01.19 | 3 | Low power design principles | 1(127-131) |
| 18 | 21.01.19 | 2 | Problems on Static and Dynamic CMOS Design | 1(94-97) |
| **UNIT III - Introduction to Sequential Logic Circuits** | | | | **Target Periods :09** |
| 19 | 28.01.19 | 2 | Static and Dynamic Latches and Registers | 1(158-160)<br>2(161-164) |
| 20 | 29.01.19 | 1 | Timing Issues, | 1(161-172) |
| 21 | 31.01.19 | 3 | Clock Strategies | 1(173-176)<br>2(164-184) |
| 22 | 01.02.19 | 2 | Memory Architecture and Memory Control Circuits | 1(176-178)<br>2(185-202) |
| 23 | 02.02.19 | 2 | Low Power Memory Circuits | 1(216-223)<br>2(285-293) |
| 24 | 04.02.19 | 2 | Synchronous Design | 2(223-229)<br>1(223-239) |
| 25 | 05.02.19 | 1 | Asynchronous Design | 1(247-249) |
| 26 | 07.02.19 | 3 | Asynchronous Design-Contd | Material |
| 27 | 08.02.19 | 2 | Pipelines | Material |
| **UNIT IV - Introduction to Designing Arithmetic Building Blocks** | | | | **Target Periods :09** |
| 28 | 18.02.19 | 2 | Data Path Circuits | 1(285-287)<br>2(360-365) |
| 29 | 19.02.19 | 1 | Architectures For Ripple Carry Adders | |
| 30 | 21.02.19 | 3 | Multipliers | 1(287-302) |
| 31 | 22.02.19 | 2 | Manchester carry chain adder | 1(305-307) |
| 32 | 23.02.19 | 3 | Carry Look Ahead Adders | 1(308-309) |
| 33 | 25.02.19 | 2 | Dividers | 1(305-307) |
| 34 | 26.02.19 | 1 | High Speed Adders | 1(311-313) |
| 35 | 28.02.19 | 3 | Accumulators | 1(326-327) |
| 36 | 01.03.19 | 2 | Speed And Area Tradeoff | 1(328-329) |
| UNIT V - Introduction to Implementation Strategies | | | Target Periods:09 | |
| 37 | 07.03.19 | 3 | ASIC | 1(285-287) |
| 38 | 08.03.19 | 2 | Full custom and Semi custom design | 1(361-367) |
| 39 | 09.03.19 | 2 | Standard Cell Design | 1(381-405) |
| 40 | 11.03.19 | 2 | Cell Libraries | 1(408-410) |
| 41 | 12.03.19 | 1 | FPGA | 1(337-340) |
| 42 | 14.03.19 | 3 | FPGA building block architectures | 1(412-415) |
| 43 | 15.03.19 | 2 | FPGA Interconnect | 1(419-421) |

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

| | | | | |
|---|---|---|---|---|
| 44 | 16.03.19 | 1 | Routing Procedures | [illegible] |
| 45 | 18.03.19 | 2 | Routing Procedures-Contd | [illegible] |
| Content Beyond the Syllabus | | | | |
| 46 | | | Scan based test techniques | Material |
| 47 | | | Application Specific Integrated Circuits | Material |

**Book Reference - Text Books**

| Sl. | Title of the Book | Author | Publisher | Year |
|---|---|---|---|---|
| 1. | Digital Integrated Circuits: A Design Perspective | Jan Rabaey, Anantha Chandrakasan, B.Nikolic | Prentice Hall of India | 2003 |
| 2. | Application Specific Integrated Circuits | M.J. Smith | Addisson Wesley | 1997 |

**Book Reference – References**

| Sl | Title of the Book | Author | Publisher | Year |
|---|---|---|---|---|
| 1. | Principles of CMOS VLSI Design | N.Weste. K.Eshraghian | Addision Wesley | 1993 |
| 2. | CMOS Circuit Design, Layout and Simulation | R.Jacob Baker, Harry W.Li., David E.Boyee | Prentice Hall of India | 2005 |
| 3. | BASIC VLSI Design | A.Pucknell, Kamran Eshraghian | Prentice Hall of India | 2005 |

**Website Reference:**
http://nptel.iitm.ac.in/courses.php?branch=Electrical
www.freebookspot.com

M. Manthri
Signature of the Faculty in-charge

N. Nagathi
HoD ECE

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## Identification of Curricular Gap & Content Beyond Syllabus(CBS)

**Name of the Faculty :Ms.M.Nandhini** **Course Code & Name:EC 6601&VLSI Design**

**Degree & Program:B.E. /ECE** **Semester & Section: III / B** **Academic Year: 2018 -2019 /EVEN**

**I.Mapping of Course Outcomes with POs & PSOs.( before CBS)**

**Table.1 Mapping of COs, C, PSOs with POs - before CBS.**

| Course | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C304.1 | 2 | 2 | 2 | 2 | - | - | - | - | - | - | 1 | 2 | 3 | 3 |
| C304.2 | 2 | 2 | 2 | 2 | - | - | - | - | - | - | 1 | 1 | 3 | 3 |
| C304.3 | 2 | 2 | 2 | 2 | - | - | - | - | - | - | 1 | 2 | 3 | 3 |
| C304.4 | 2 | 2 | 2 | 2 | - | - | - | - | - | - | 1 | 3 | 3 | 3 |
| C304.5 | 2 | 2 | 2 | 2 | - | - | - | - | - | - | 1 | 2 | 3 | 3 |
| C304.6 | 2 | 2 | 2 | 2 | - | - | - | - | - | - | 1 | 2 | 3 | 3 |

**II. Identification of content beyond syllabus.**

**Table.2 Identification of content beyond syllabus**

| Details of Content Beyond Syllabus(CBS) added | POs strengthened/ vacant filled | CO/Unit |
|---|---|---|
| Scan based test techniques | | 5 |
| Application Specific Integrated Circuits | | 5 |

**III. Mapping of Course Outcomes with POs & PSOs. (After CBS)**

**Table.3 Mapping of COs, C, PSOs with POs- after CBS.**

| Course | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C304.1 | 2 | 2 | 2 | 2 | - | - | - | - | - | - | 1 | 2 | 3 | 3 |
| C304.2 | 2 | 2 | 2 | 2 | - | - | - | - | - | - | 1 | 1 | 3 | 3 |
| C304.3 | 2 | 2 | 2 | 2 | - | - | - | - | - | - | 1 | 2 | 3 | 3 |
| C304.4 | 2 | 2 | 2 | 2 | - | - | - | - | - | - | 1 | 3 | 3 | 3 |
| C304.5 | 2 | 2 | 2 | 2 | 2 | - | - | - | - | - | 1 | 2 | 3 | 3 |
| C304.6 | 2 | 2 | 2 | 2 | - | - | - | - | - | - | 1 | 2 | 3 | 3 |
| C304 | 2 | 2 | 2 | 2 | 2 | - | - | - | - | - | 1 | 2 | 3 | 3 |

M. Nandhini
**Signature of the Faculty**

N. Vinayagam
**HoD/ECE**

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

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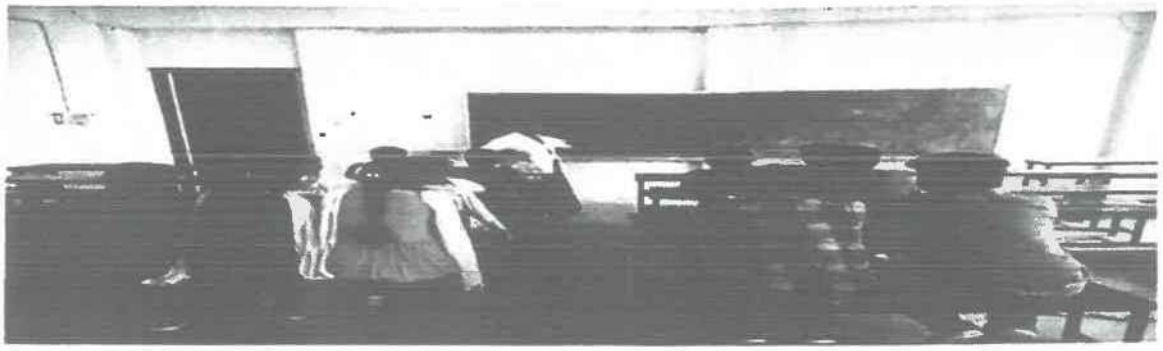
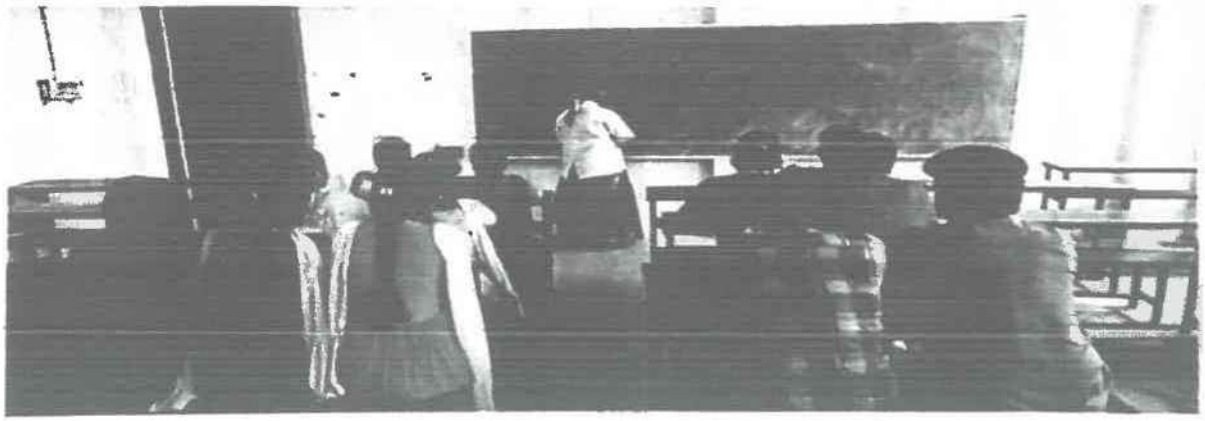
## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## Proof of Curricular Gap & Content Beyond Syllabus(CBS)

**Name of the Faculty :Ms.M.Nandhini**
**Degree & Program:B.E. /ECE**
**Academic Year: 2018 -2019 /EVEN**

**Course Code & Name:EC6601- VLSI DESIGN**
**Semester & Section: VI / B**





M. Nandhini
**Signature of the Faculty**

Nirgath
**HoD/ECE**

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## Assignment Question Paper

| Assignment – 01 | | | Date of Issue: | 04.01.2019 | Marks | 10 |
|---|---|---|---|---|---|---|
| Course code | EC6601 | Course Title | VLSI DESIGN | | | |
| Year | III | Semester/Section | VI/ B | Date of Submission: | 11.01.2019 | |

| Q.No | Questions | CO |
|---|---|---|
| 1 | Explain the characteristics of Pass Transistor and Transmission gate | C304.2 |
| 2 | Explain the static and dynamic power dissipation | C304.2 |

M.Nandhini.

**Name and Signature of the Faculty Incharge**

(M.Nandhini)

N.Jyothi

**HoD/ECE**

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## Assignment Answer Sheet

**Name of the Student :**

**AU Register Number:**

| Assignment – 01 | | | Date of Issue: | 04.01.2019 | Marks | 10 |
|---|---|---|---|---|---|---|
| Course code | EC6601 | Course Title | VLSI Design | | | |
| Year | III | Semester/Section | VI/ B | Date of Submission: | 11.01.2019 | |

| Q.No | Questions | CO |
|---|---|---|
| 1 | Explain the characteristics of Pass Transistor and Transmission gate | C304.2 |
| 2 | Explain the static and dynamic power dissipation | C304.2 |

### Mark Allocation

| Rubrics | Marks Allocated | Marks obtained |
|---|---|---|
| Content Quality | 6 | 5 |
| Presentation Quality | 2 | 1 |
| Timely submission | 2 | 2 |
| Total marks | 10 | 8 |

M. Nandini

**Name and Signature of the Faculty Incharge**

(M. Nandini)

N Vijayalakshmi

**HoD/ECE**

Register Number:

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**Internal Assessment Exam - I**

| | | | | | | |
|---|---|---|---|---|---|---|
| Course code | EC6601 | Course Title | VLSI DESIGN | Date/Session | 24.01.2019 | Marks 50 |
| Regulation | 2022 | Duration | 90 minutes | Academic Year | 2018-19 | |
| Year | III | Semester | VI | Department | ECE | |

**COURSE OUTCOMES**

| | |
|---|---|
| CO1: | In depth knowledge of MOS technology |
| CO2: | Explain the Combinational Logic Circuits and Design Principles |
| CO3: | Explain Sequential Logic Circuits and Clocking Strategies |
| CO4: | Explain the Memory architecture and building blocks |
| CO5: | Apply the ASIC Design Process and Testing |
| CO6: | Design using Programmable Devices (ROM, PLA, FPGA), |

| Q.No. | Question | CO | BTS |
|---|---|---|---|
| | **PART A** (Answer all the Questions 10 x 2 = 20 Marks) | | |
| 1 | Define Elmore constant | CO2 | K1 |
| 2 | Give the different symbols for transmission gate. | CO2 | K1 |
| 3 | What are the methods available to reduce dynamic power dissipation? | CO2 | K3 |
| 4 | Draw 2 input XNOR gate using nmos pass transistor | CO2 | K1 |
| 5 | What is meant by domino and pseudo nmos logic | CO2 | K1 |
| 6 | Implement a 2:1 multiplexer using pass transistor | CO2 | K1 |
| 7 | Draw 2 input XOR gate using nmos pass transistor | CO2 | K3 |
| 8 | What is transmission gate? | CO2 | K1 |
| 9 | List the sources of static and dynamic power dissipation | CO2 | K3 |
| 10 | What is dynamic power dissipation? | CO2 | K1 |
| | **PART B** (Answer all the Questions 2 x 10 = 20 Marks) | | |
| 11a | Discuss in detail about RC delay model and Elmore delay model | CO2 | K2 |
| | OR | | |
| 11b | Explain in detail with neat diagram about SFPL &CVSL | CO2 | K3 |
| 12a | Write neat diagram for an expression Y=(AB+(C+D)(DE)' | CO2 | K1 |
| | OR | | |
| 12b | Write neat diagram for an expression Y=(A+B)+(C+D)(D+E)' | CO2 | K2 |
| | **PART C** (Answer all the Questions 1 x 10 = 10 Marks) | | |
| 13a | Realize a 2 input NOR gate using static CMOS logic,Domino logic and pseudo nmos logic (or) | CO2 | K3 |
| | OR | | |
| 13b | Design a half adder using static CMOS logic<br>Design a 4:1 MUX using 2:1 MUX. Realize it using transmission gate. | CO2 | K4 |

M. Vanathi

Course Faculty

(Name /Sign / Date)

M. Nandhini

24/1/2019

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

N Bagthi

HOD

(Name /Sign / Date)

N. Vaijayanthi

24/1/2019

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Internal Assessment Test Answer Book

| Name | S. Anushya | | | Year/ Semester/Section | III / VI / B |
|---|---|---|---|---|---|
| Batch No. | 8112161060 | Date/Session | 24.01.19 FN | Department | ECE |
| Course code | EC 6601 | Course Title | VLSI Design | | |
| Internal Assessment Test | IAT 1 ☐ | IAT 2 ☑ | IAT 3 ☐ | Model ☐ | |
| Name and Signature of the Invigilator with date | M. Bhuvaneshwari | | | | |

Instruction to the Student: Put tick mark to the question attended in the column against question.

| Part A | | | Part B / Part C | | | | | Total Marks |
|---|---|---|---|---|---|---|---|---|
| Q. No. | ✓ | Marks | Q. NO. | ✓ | a Marks | ✓ | b Marks | |
| 1 | | 1 | 11 | | 09 | | | |
| 2 | | 1 | 12 | | 7 | | | |
| 3 | | 2 | 13 | | | | 8 | |
| 4 | | 2 | 14 | | | | | |
| 5 | | 2 | 15 | | | | | |
| 6 | | 1 | 16 | | | | | |
| 7 | | 2 | | | | Total | | 24 |
| 8 | | — | 38/50 | | | | | |
| 9 | | 2 | | | | | | |
| 10 | | 1 | | | | | | |
| Total | | 14 | Grand Total | | | | | |

M. Nandhini (M. Nandhini)
Name and Signature of the Examiner with date (26/1/2019)

| To be filled by the examiner | | | | | | | |
|---|---|---|---|---|---|---|---|
| Course Outcomes | 1 | 2 | 3 | 4 | 5 | 6 | Total |
| Marks allotted | | 50 | | | | | |
| Marks Obtained | | 38 | | | | | |

**IQAC Audit - Remarks**

Try to get high marks

Nivedhi
Name and Signature of the IQAC member

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
M... [illegible] 620 012.

# INDRA GANESAN COLLEGE OF ENGINEERING

IG VALLEY, MANIDANDAM, TIRUCHIRAPPALLI – 620012

DEPARTMENT OF ECE

..CADEMIC YEAR 2018 – 2019 (EVEN SEMESTER)

**STUDENTS MARK STATEMENT- CO BASED**

CYCLE TEST-II

SUBJECT CODE &TITLE: EC6601 & VLSI DESIGN

YEAR/SEM: III/VI MONTH & YEAR:01/2019

| S.NO | REG NO | STUDENT NAME | CO2 | Retest CO2 | TOTAL 60 | TOTAL (100) |
|---|---|---|---|---|---|---|
| 1 | Abarna T | 811216106001 | 40 | | 40 | 67 |
| 2 | Amsavalli S | 811216106002 | 52 | | 52 | 87 |
| 3 | Anushya S | 811216106003 | 42 | | 42 | 70 |
| 4 | Arockia Nivetha S | 811216106004 | 38 | | 38 | 63 |
| 5 | Ashefa N | 811216106005 | 35 | | 35 | 58 |
| 6 | Dhanalakshmi T | 811216106006 | AB | 35 | 35 | 58 |
| 7 | Femina Begum A | 811216106008 | 38 | | 38 | 63 |
| 8 | Gayathri J | 811216106009 | 35 | | 35 | 58 |
| 9 | Joysefshiba J | 811216106010 | 32 | | 32 | 53 |
| 10 | Keerthana P | 811216106011 | 48 | | 48 | 80 |
| 11 | Keerthana S | 811216106012 | 40 | | 40 | 67 |
| 12 | Keerthika D | 811216106013 | 38 | | 38 | 64 |
| 13 | Lathasri S | 811216106014 | 48 | | 48 | 80 |
| 14 | Menaka R | 811216106015 | 52 | | 52 | 87 |
| 15 | Mithra P | 811216106016 | 32 | | 32 | 53 |
| 16 | Mohan Raj S | 811216106017 | 35 | | 35 | 58 |
| 17 | Nilavar Nisha F | 811216106018 | 32 | | 32 | 53 |
| 18 | Pavithra P | 811216106019 | 8 | 30 | 30 | 50 |
| 19 | Pavithra V | 811216106020 | 40 | | 40 | 67 |
| 20 | Prabhu A | 811216106021 | 45 | | 45 | 75 |
| 21 | Preetha M | 811216106022 | 45 | | 45 | 75 |
| 22 | Prema S | 811216106024 | 45 | | 45 | 75 |
| 23 | Raahul BN | 811216106025 | 40 | | 40 | 67 |
| 24 | Ramya S | 811216106026 | 45 | | 45 | 75 |
| 25 | Ruban Raj S | 811216106027 | 48 | | 48 | 80 |
| 26 | Saranya M | 811216106028 | 35 | | 35 | 58 |
| 27 | Saravanan S | 811216106030 | 40 | | 40 | 67 |
| 28 | Shanakya P | 811216106031 | 48 | | 48 | 80 |
| 29 | Sorna J | 811216106032 | 35 | | 35 | 58 |
| 30 | Sudharsan K | 811216106033 | 30 | | 30 | 50 |
| 31 | Suvathi R | 811216106034 | 42 | | 42 | 70 |
| 32 | Swathi S | 811216106035 | 48 | | 48 | 80 |
| 33 | Udaya Rani K | 811216106036 | 30 | | 30 | 50 |
| 34 | Vettai P | 811216106037 | 35 | | 35 | 58 |

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
[illegible] Trichy-620 012.

**MARKS RANGE:**

| <20 | 20-30 | 31-40 | 41-50 | 51-60 | 61-70 | 71-80 | 81-90 | 91-100 |
|---|---|---|---|---|---|---|---|---|
| | | | 03 | 10 | 10 | 9 | 2 | |

| | |
|---|---|
| **Total No.of Candidates Present** | 33 |
| **Total No.of Candidates Absent** | 01 |
| **Total No.of Students Pass** | 32 |
| **Total No. of Students Fail** | 01 |
| **Percentage of Pass** | 98 |

M. Nandhini
**STAFF INCHARGE**

N. Vijayashri
**HoD/ECE**

**PRINCIPAL**

Dr. G. Balakrishnan, M.E., Ph.D.
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

# INDRA GANESAN COLLEGE OF ENGINEERING

IG Valley, Manikandam, Tiruchirappalli, Tamil Nadu – 620 012, India

(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### ROOT CAUSE ANALYSIS

**Name of the Faculty** :Ms.M.Nandhini
**Degree & Program** :B.E &ECE
**IA Test** : II
**Target** : 100 %

**Course Code & Name** :EC 6601&VLSI Design
**Semester & Section** :VI&B
**University Exam/Month & Year**:APR-MAY 2019
**Achieved** : 98 %

| S.NO | BATCH NO | NAME OF THE STUDENT | CAUSES FOR FAILURE | SIGNATURE OF THE STUDENT WITH DATE | CORRECTIVE ACTION TAKEN | PREVENTIVE ACTION TAKEN | FOLLOWUP STATUS | REMARKS OF THE HOD |
|---|---|---|---|---|---|---|---|---|
| 1. | 811216106006 | DHANALAKSHMI T | WENT TO DEATH | T.Dhanalakshmi 5/12/19 | RETEST | ADVISED | PROGRESS MONITORED | |
| 2. | 811216106019 | PAVITHRA P | FEVER. | Pavithra 5/12/19 | RETEST | ADVISED | PROGRESS MONITORED | |

M.Nandhini
**Signature of the Faculty Member**

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

N.Vijayalakshmi
**Signature of the HoD/ECE**

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(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

## IQAC Academic Audit Form

ACADEMIC YEAR: 2018-2019 ODD / EVEN SEMESTER

| Name of Department : | ECE | Year / Sem / Sec : | 2 / III / A | No. of Students Registered : | 120 |
|---|---|---|---|---|---|
| Details of Examination : | IA Test -1 / IA Test -2 / IA Test -3 / Model Test | | | | |

| S.No. | Course Code | List of Reg.No Verified | Course Log Book Verified (Y / N) | Course File Verified (Y / N) | No of students Attended | No of Absentees | No of Failures | Pass % | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| 1. | MG6851 | 811216106001 | Y | Y | 50 | 01 | 8 | 84 | Try to get 100/= Percent |
| 2 | CS6303 | 811216106005 | Y | Y | 51 | – | 4 | 92 | Presentation clear. |
| 3 | CS6551 | 811216106013 | Y | Y | 50 | 1 | 5 | 90 | Content ok |
| 4 | EC6601 | 811216106025 | Y | Y | 50 | 1 | 1 | 98 | Presentation File |
| 5 | EC6602 | 811216106026 | Y | Y | 48 | 3 | 4 | 92 | Try to get 100% |
| 6. | EC6001 | 811216106030 | Y | Y | 51 | – | 3 | 94 | Pass percentage improve |

**Verified by**

| | |
|---|---|
| **External Member Name and Signature:** | N. Vaijayanthi |
| **Internal Member Name and Signature:** | M. Nandhini |

Overall Remarks:

N. Vaggthi
HoD/ ECE

N. Vaggthi
IQAC Co-ordinator

Principal

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
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Manikandam, Trichy-620 012.

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## Identification of Curricular Gap & Content Beyond Syllabus(CBS) Material

# Scan-Based Techniques

The controllability and observability can be enhanced by providing more accessible logic nodes with use of additional primary input lines and multiplexors.However, the use of additional I/O pins can be costly not only for chip fabrication but also for packaging. A popular alternative is to use scan registers with both shift and parallel load capabilities. The scan design technique is a structured approach to design sequential circuits for testability. The storage cells in registers are used as observation points, control points, or both. By using the scan design techniques, the testing of a sequential circuit is reduced to the problem of testing a combinational circuit.

In general, a sequential circuit consists of a combinational circuit and some storage elements. In the scan-based design, the storage elements are connected to form a long serial shift register, the so-called scan path, by using multiplexors and a mode (test/ normal) control signal, as shown in Fig. 1 .

In the test mode, the scan-in signal is clocked into the scan path, and the output of the last stage latch is scanned out. In the normal mode, the scan-in path is disabled and the circuit functions as a sequential circuit. The testing sequence is as follows:

Step 1: Set the mode to test and, let latches accept data from scan-in input.
Step 2: Verify the scan path by shifting in and out the test data.
Step 3: Scan in (shift in) the desired state vector into the shift register.
Step 4: Apply the test pattern to the prim ary input pins.
Step 5: Set the mode to normal and observe the primary outputs of the circuit after sufficient time for propagation.,
Step 6: Assert the circuit clock, for one machine cycle to capture the outputs of the combinational logic into the registers.
Step 7: Return to test mode; scan out the contents of the registers, and at the same time scan in the next pattern.
Step 8: Repeat steps 3-7 until all test patterns are applied.

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

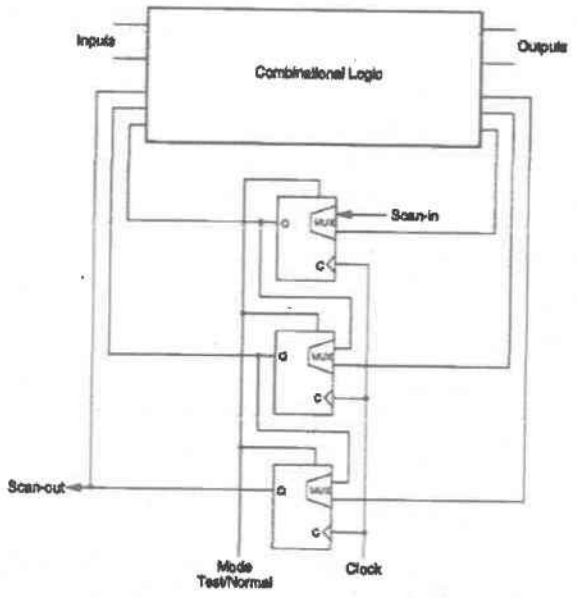



**Figure 1: The general structure of scan-based design**

The storage cells in scan design can be implemented using edge-triggered D flipflops, master-slave flip-flops, or level-sensitive latches controlled by complementary clock signals to ensure race-free operation. Figure 2 shows a scan-based design of an edge-triggered D flip-flop. In large high-speed circuits, optimizing a single clock signal for skews, etc., both for normal operation and for shift operation, is difficult. To overcome this difficulty, two separate clocks, one for normal operation and one for shift operation, are used. Since the shift operation does not have to be performed at the target speed, its clock is much less constrained.

An important approach among scan-based designs is the level sensitive scan design (LSSD), which incorporates both the level sensitivity and the scan path approach using shift registers. The level sensitivity is to ensure that the sequential circuit response is independent of the transient characteristics of the circuit, such as the component and wire delays. Thus, LSSD removes hazards and races. Its ATPG is also simplified since tests have to be generated only for the combinational part of the circuit.

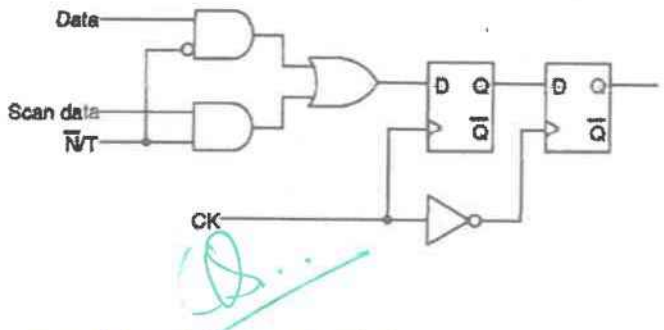


**Figure 2 : Scan-based design of an edge-triggered D flip-flop**

The boundary scan test method is also used for testing printed circuit boards (PCBs) and multichip modules (MCMs) carrying multiple chips. Shift registers are placed in each chip close to I/O pins in order to form a chain around the board for testing. With successful implementation of the boundary scan method, a simpler tester can be used for PCB testing.

On the negative side, scan design uses more complex latches, flip-flops, I/O pins, and interconnect wires and, thus, requires more chip area. The testing time per test pattern is also increased due to shift time in long registers

# Application-specific integrated circuit

An application-specific integrated circuit (ASIC /ˈeɪsɪk/) is an integrated circuit (IC) chip customized for a particular use, rather than intended for general-purpose use, such as a chip designed to run in a digital voice recorder or a high-efficiency videocodec. Application-specific standard product chips are intermediate between ASICs and industry standard integrated circuits like the 7400 series or the 4000 series.

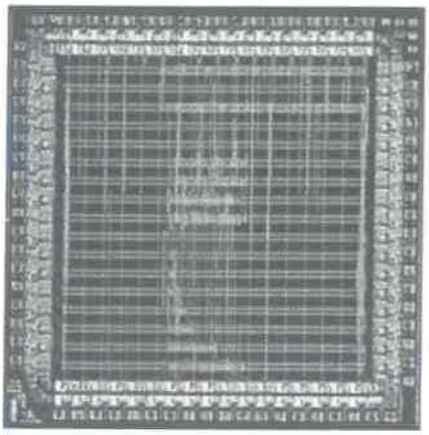
[1] ASIC chips are typically fabricated using metal–oxide–semiconductor (MOS) technology, as MOS integrated circuit chips.

[2]As feature sizes have shrunk and chip design tools improved over the years, the maximum complexity (and hence functionality) possible in an ASIC has grown from 5,000 logic gates to over 100 million. Modern ASICs often include entire microprocessors, memory blocks including ROM, RAM, EEPROM, flash memory and other large building blocks.

Such an ASIC is often termed a SoC (system-on-chip). Designers of digital ASICs often use a hardware description language (HDL), such as Verilog or VHDL, to describe the functionality of ASICs.

[1]Field-programmable gate arrays (FPGA) are the modern-day technology improvement on breadboards, meaning that they are not made to be application-specific as opposed to ASICs. Programmable logic blocks and programmable interconnects allow the same FPGA to be used in many different applications. For smaller designs or lower production volumes, FPGAs may be more cost-effective than an ASIC design, even in production. The non-recurring engineering (NRE) cost of an ASIC can run into the millions of dollars. Therefore, device manufacturers typically prefer FPGAs for prototyping and devices with low production volume and ASICs for very large production volumes where NRE costs can be amortized across many devices.[3]

## Gate-array and semi-custom design



Microscope photograph of a gate-array ASIC showing the predefined logic cells and custom interconnections. This particular design uses less than 20% of available logic gates.

Gate array design is a manufacturing method in which diffused layers, each consisting of transistors and other active devices, are predefined and electronics wafers containing such devices are "held in stock" or unconnected prior to the metallization stage of the fabrication process. The physical design process defines the interconnections of these layers for the final device. For most ASIC manufacturers, this consists of between two and nine metal layers with each layer running perpendicular to the one below it. Non-recurring engineering costs are much lower than full custom designs, as photolithographic masks are required only for the metal layers. Production cycles are much shorter, as metallization is a comparatively quick process; thereby accelerating time to market.

Gate-array ASICs are always a compromise between rapid design and performance as mapping a given design onto what a manufacturer held as a stock wafer never gives 100% circuit utilization. Often difficulties in routing the interconnect require migration onto a larger array device with a consequent increase in the piece part price. These difficulties are often a result of the layout EDA software used to develop the interconnect.

Pure, logic-only gate-array design is rarely implemented by circuit designers today, having been almost entirely replaced by field-programmable devices. The most prominent of such devices are field-programmable gate arrays (FPGAs) which can be programmed by the user and thus offer minimal tooling charges, non-recurring engineering, only marginally increased piece part cost, and comparable performance.

Today, gate arrays are evolving into structured ASICs that consist of a large IP core like a CPU, digital signal processor units, peripherals, standard interfaces, integrated memories, SRAM, and a block of reconfigurable, uncommitted logic. This shift is largely because ASIC devices are capable of integrating large blocks of system functionality, and systems on a chip (SoCs) require glue logic, communications subsystems (such as networks on chip), peripherals, and other components rather than only functional units and basic interconnection.

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.

In their frequent usages in the field, the terms "gate array" and "semi-custom" are synonymous when referring to ASICs. Process engineers more commonly use the term "semi-custom", while "gate-array" is more commonly used by logic (or gate-level) designers.

Dr. G. Balakrishnan, M.E., Ph.D.,
Principal
Indra Ganesan College of Engineering
IG Valley, Madurai Main Road
Manikandam, Trichy-620 012.